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Investigation of Electronic and Opto-electronic Properties of Two-dimensional Layers (2D) of Copper Indium Selenide Field Effect Transistors

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INVESTIGATION OF ELECTRONIC AND OPTO-ELECTRONIC PROPERTIES OF TWO-DIMENSIONAL (2D) LAYERS OF COPPER INDIUM SELENIDE FIELD EFFECT TRANSISTORS

by

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A Thesis Submitted in
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for the Degree of Master of Science in the field of Physics

Approved by:

Prof. Saikat Talapatra

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TITLE: INVESTIGATION OF ELECTRONIC AND OPTO-ELECTRONIC PROPERTIES OF TWO-DIMENSIONAL LAYERS (2D) OF COPPER INDIUM SELENIDE FIELD EFFECT TRANSISTORS

MAJOR PROFESSOR: Prof. Saikat Talapatra.

Investigations performed in order to understand the electronic and optoelectronic properties of field effect transistors based on few layers of 2D Copper Indium Selenide **(**$CuIn_7Se_{11}$) are reported. In general, field effect transistors (FETs), electric double layer field effect transistors (EDL-FETs), and photodetectors are crucial part of several electronics based applications such as tele-communication, bio-sensing, and opto-electronic industry. After the discovery of graphene, several 2D semiconductor materials like TMDs (MoS_2, WS_2, and $MoSe_2$ etc.), group III-VI materials (InSe, GaSe, and SnS_2 etc.) are being studied rigorously in order to develop them as components in next generation FETs. Traditionally, thin films of ternary system of Copper Indium Selenide have been extensively studied and used in optoelectronics industry as photoactive component in solar cells. Thus, it is expected that atomically thin 2D layered structure of Copper Indium Selenide can have optical properties that could potentially be more advantageous than its thin film counterpart and could find use for developing next generation nano devices with utility in opto/nano electronics.

Field effect transistors were fabricated using few-layers of $CuIn_7Se_{11}$ flakes, which were mechanically exfoliated from bulk crystals grown using chemical vapor transport technique. Our FET transport characterization measurements indicate n-type behavior with electron field effect mobility $\mu_{FE} \approx 36$ cm^2 V^{-1} s^{-1} at room temperature when Silicon dioxide (SiO_2) is used as a back gate. We found that in such back gated field effect transistor an on/off ratio of ~ 10^4 and a

subthreshold swing ≈ 1 V/dec can be obtained. Our investigations further indicate that Electronic performance of these materials can be increased significantly when gated from top using an ionic liquid electrolyte [1-Butyl-3-methylimidazolium hexafluorophosphate (BMIM-PF_6)]. We found that electron field effect mobility μ_{FE} can be increased from ~ 3 cm^2 V^{-1} s^{-1} in SiO2 back gated device to ~ 18 cm^2 V^{-1} s^{-1}in top gated electrolyte devices. Similarly, subthreshold swing can be improved from ~ 30 V/dec to 0.2 V/dec and on/off ratio can be increased from 10^2 to 10^3 by using an electrolyte as a top gate.

These FETs were also tested as phototransistors. Our photo-response characterization indicate photo-responsivity ~ 32 A/W with external quantum efficiency exceeding 10^3 % when excited with a 658 nm wavelength laser at room temperature. Our phototransistor also exhibit response times ~ tens of μs with specific detectivity (D*) values reaching ~ 10^{12} Jones. The $CuIn_7Se_{11}$ phototransistor properties can be further tuned and enhanced by applying a back gate voltage along with increased source drain bias. For example, photo-responsivity can gain substantial improvement up to ~ 320 A/W upon application of a gate voltage (V_g = 30 V) and/or increased source-drain bias. The photo-responsivity exhibited by these photo detectors are at least an order of magnitude better than commercially available conventional Si based photo detectors coupled with response times that are orders of magnitude better than several other family of layered materials investigated so far. Further photocurrent generation mechanisms, effect of traps is discussed in detail.

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- Prasanna Dnyaneshwar Patil

DEDICATION

This thesis is proudly dedicated to…

आई and आण्णा

My dear grandparents!!

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CHAPTER 1

INTRODUCTION AND MOTIVATION

Mid-20th century is considered as physical foundation of virtual world which correspond to birth of semiconductor electronics. In 1947 at Bell Labs, John Bardeen, William Shockley, and Walter Brattain designed semiconductor transistor for the first time, revolutionizing the field of electronics and laying the foundation of the Information Age. Bardeen, Brattain, and Shockley shared the 1956 Nobel Prize in Physics for their research on semiconductor and discovery of transistor [1]. After a decade later, Jack Kilby of Texas Instruments invented and built first integrated circuit and was awarded a Nobel Prize in Physics in 2000 [2].

Around the same time, Richard Feynman gave his famous lecture titled 'There's Plenty of Room at the Bottom' at an American Physical Society meeting, California Institute of Technology, which is considered as first lecture in technology and engineering at the atomic scale [3]. Thus opening the doors for the field of nanotechnology and several other interesting phenomenon & physics at nano scale. Few years later, Intel co-founder Gordon Moore predicted several trends in the field of electronics [4]. One of well-known trend is 'Moore's Law' which state that number of transistor on an integrated circuit (IC) will double every year (later revised to every 2 years) and this growth rate will continue for another decade. Trend that Moore envisioned has continued for next half a century and it is attributed to rise of nanotechnology as transistors have approached to atomic dimensions.

1980s saw initial development towards nanoscale materials when Russia's Alexei Ekimov discovered semiconducting quantum dots in glass matrix exhibiting good electronic and optical properties [5]. Couple of years later, researchers at Rice University, Harold Kroto, Sean O'Brien, Robert Curl, and Richard Smalley discovered Buckminsterfullerene (or bucky-ball),

C_{60}, composed entirely of carbon. The team was awarded the 1996 Nobel Prize in Chemistry [6].

In 1991, Sumio Iijima of NEC Corp. reported observation of multi-walled carbon nanotubes (MW-CNTs) [7]. Two years later, independently Iijima and Ichihashi [8] and Bethune et al. [9] reported the growth of single-walled carbon nanotubes (SW-CNTs) in the same issue of Nature. Impact of these articles was tremendous on scientific community as nanoscience and nanotechnology gained momentum. However Radushkevich and Lukyanovich [10] reported first direct observation of MW-CNTs in 1952 and Oberlin et al. [11] published an image of SW-CNTs in 1976. Apart from controversy surrounding discovery of CNTs, extraordinary mechanical, electrical, and thermal properties combined with a low density of CNTs has revolutionize materials at low dimensions. Quantum dots (0D) and nanotubes (1D) were main area of focus until, in 2004 researchers at University of Manchester, Andre Geim and Konstantin Novoselov showed groundbreaking experiments regarding the two-dimensional (2D) material graphene [12] and they shared 2010 the Nobel Prize in Physics.

1.1 Two-Dimensional materials

Graphene, a single atomic layer of carbon, was first material in class of Two-dimensional (2D) materials which was studied rigorously [13-15]. Various unique properties of graphene made it material of interest among several researchers for fundamental studies and future applications. Theoretically, density of graphene is estimated as 0.77 mg/m^2 thus hypothetically a sheet of graphene measuring 1 m^2 as area would weight 0.77 mg. Graphene absorbs only 2.3% of light intensity irrespective of wavelength, thus making it almost transparent. Graphene has a stiffness / breaking strength of 42 N/m. In order to put it in perspective, steel film of same thickness as graphene will have 2D breaking strength of 0.08-0.40 N/m, thus graphene is 100 times stronger than strongest steel. Theoretically, mobility limited by acoustic phonons is

estimated to be 200,000 $cm^2 V^{-1} s^{-1}$ at carrier density of 10^{12} cm^{-2} and the 2D sheet resistivity to be 31 Ω/m^2. Also, 2D confinement of electron in graphene gives rise to quantum hall effect. Thermal conductivity of graphene was measured to be ~ 5000 $W m^{-1} K^{-1}$ which is 10 times better than that of copper (401 $W m^{-1} K^{-1}$). Thus graphene can be used as strong flexible conductor [16].

The high carrier mobility observed in graphene devices suggested that it would be a perfect material for electronics, particularly for transistor applications and will be a successor of traditional semiconductor. As graphene transistor research progressed thoroughly, it became evident that graphene would not be a good fit as it does not possess a bandgap, which is essential for proper transistor operation. Although graphene is band gapless, research have shown that bandgap can be opened by modification. Popular technique to open a bang gap by creating graphene nanoribbons (GNRs) by either chemical synthesis [17,18] or lithography patterning [19,20]. It has been observed that band gap increased with decreasing width of ribbon. A band gap of 0.4 eV can be achieved by ribbons of width less than 10 nm. One of the main drawbacks of using this technique is lack of control over graphene edges leading to non-universal properties. Another technique for opening band gap is by applying electric field perpendicular to bi-layer graphene (BLG) [21,22]. It was seen that conduction and valence band of BLG are Mexican-hat shaped and not parabolic like other semiconductors [21]. A band gap of 0.13 eV can be accomplished using this technique, though it is not sufficient for transistor application [22].

As interest in graphene as material for transistor began to decline, in 2011, Andras Kis *et al.*, [23] demonstrated fabrication of single layer MoS_2 Field effect transistor (FET). With this finding the research on 2D materials for electronics gained a massive momentum. Over a short

period of time, a new class of 2D materials emerged and a number of research groups started on working on non-graphene based 2D FETs. This number has steadily increased since 2011 and in 2011, the ITRS (International Technology Roadmap for Semiconductor), has mentioned 2D materials beyond graphene as future candidates for electronics.

Recent advances in synthesis techniques of 2D materials have also set foundations for discovering new atomically thin layered materials with exotic functionalities. Currently a family of 2D materials consists of wide selections of composition incorporating most of the elements from periodic table and these are either experimentally synthesized and analyzed or computationally predicted and studied [24]. These 2D materials consists of rich variety optoelectronics properties, from metals (VS_2), semimetals (graphene) to insulators (h-BN) and semiconductors with direct and indirect band gap ranging from infrared (TMDs like $MoTe_2$, WTe_2, TiS_2), Visible (TMDs like MoS_2, WS_2 and Group III-VI materials like InSe, GaSe, GaS) to ultraviolet (germanene, SiC) range of spectrum [24]. Thus, 2D materials can potentially play a fundamental role in future optoelectronics and nanoelectronics devices, particularly towards novel ultrathin and flexible electronics.

A comprehensive research has been carried towards semiconducting transition metal dichalcogenides (TMDs) with molecular formula MX_2 where M represents transition metal (Mo, W) and X represents chalcogen (S, Se, Te) with the thickness of atomic level. TMDs can exist into two crystal structures, trigonal prismatic (denoted by 2H) and octahedral (denoted by 1T), though 2H phase is thermodynamically stable than 1T phase. Electronically, 2H phase is semiconducting whereas 1T phase is metallic [25].

Semiconducting 2H phase of TMDs have extensively studied as component for electronics [26-28]. First report on single layer MoS_2 transistors demonstrated carrier mobility of

~ 200 cm^2 V^{-1} s^{-1} and on/off ratio of ~ 10^8, by using hafnium oxide as a gate dielectric [23]. Among TMDs, WSe_2 is observed to have higher mobility of ~ 300 cm^2 V^{-1} s^{-1} in monolayer form [29]. However mobilities in TMDs based transistors are lower than mobility of commercially available Si based transistor, which has mobility of ~ 1400 cm^2 V^{-1} s^{-1}.

In case of MoS_2, monolayer has direct band gap of 1.9 eV, whereas its bulk counterpart has an indirect band gap of 1.2 eV [30]. Similar behavior has been observed in other TMDs where band gap changes from indirect to direct as number of layers thinning down from bulk to monolayers. For optoelectronics purpose, it is crucial to have direct band gap as it makes several optical process efficient. Also for absorption to be advantageous, it is desired to have longer optical path through the semiconductor material [31]. Thus, while increasing absorption of photon by increasing number of layers, advantage of direct band gap is lost. In this scenario, group III-VI based layered materials such as Indium Selenide (InSe), Gallium telluride (GaTe) etc. are thought of as materials that can provide a solution to the above mentioned issue of direct to indirect band gap transition with increasing layer thickness that occurs in TMDs.

1.2 Group III-VI layered materials

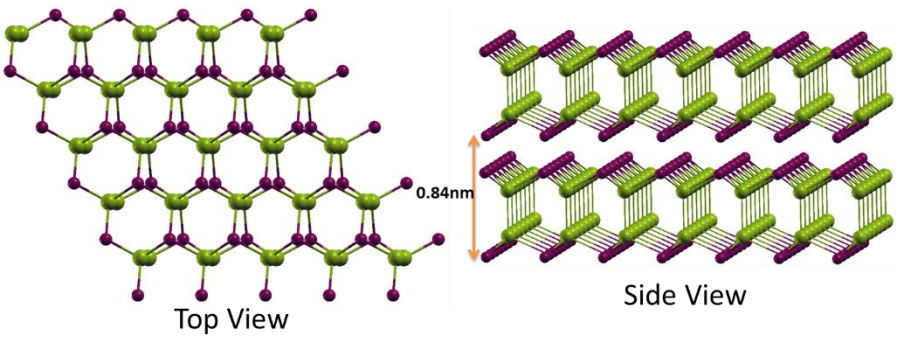

Figure 1.1: Structure of atomically thin 2D layers of InSe showing top view and side view. Thickness of one layer is approximately ~ 0.84 nm.

Group III-VI materials are another class of 2D layered materials and can be classified into two molecular formulas: MX and M_2X_3 where M represent post-transition metal from group

III (Ga, In) and X represents a chalcogen (S, Se, Te). In MX structure, let's take InSe as an example, monolayer is consist of 4 (quaternary) planer layers of closed packed Se-In-In-Se monoatomic sheets as hexagonal lattice, as shown in figure 1.1. This stacking arrangement of quaternary layers gives 4 different phase, β, ε, γ, and δ [32]. Among them, β-phase and γ-phase are commonly found in case of InSe. For β-InSe, unit cell is consist of two layers *i.e.* eight atoms whereas unit cell of γ-InSe consist of three layers *i.e.* twelve atoms [33]. Similar to TMDs, a strong covalent bonding exists within layer whereas adjacent layers are connected by weak van der Waals interactions. Thus, few layer structures of InSe can be easily acquired by standard exfoliation techniques [33]. Electronically it is observed that bulk InSe is a typical n-type semiconductor with direct band gap of 1.3 eV [34]. It has been observed that photoluminescence (PL) peaks exhibited blue shift (towards higher energy) and weakening of PL intensity as number of layers decreased to monolayer. This phenomenon correspond to direct to indirect band gap crossover with decreasing layer numbers [35] and which is an opposite trend compared to TMDs. Strikingly other MX stoichiometries like GaS, GaSe and GaTe exhibits different and complicated crystal structures, thus different electronic properties. For example bulk GaS [36] is n-type semiconductor with indirect band gap of 3.05 eV, GaSe [36] is p-type semiconductor with indirect band gap of 2.1 eV whereas bulk GaTe [37] has a direct band gap of 1.7 eV.

For M_2X_3 stoichiometry, In_2Se_3 is most studied material. It comes in tetrahedral lattice with five known crystal forms (α, β, γ, δ, and κ) [38]. γ-In_2Se_3 is distorted wurtzite like structure and δ-In_2Se_3 is monoclinic structure whereas α-In_2Se_3, β-In_2Se_3, and κ-In_2Se_3 are formed by inserting a cationic vacancy plane along *ab*-direction [39]. Most common form of In_2Se_3 are α and β phase, which has same crystallographic structure but differ in lattice parameter which governs dissimilar materials properties. Recently, transformation of α → β phase can be caused

by temperature and transformation temperature increases with decrease in layer numbers [40]. Monolayer of In_2Se_3 consists of quintuple atomic layers of Se-In-Se-In-Se, held together by strong covalent bond and adjacent layers are held together by weak van der Waals interactions. The direct band gap of α-In_2Se_3 is found to be 1.48 eV [41]. Thus, in general, Group III-VI layered materials have direct band gap structure and can be employed as high performance opto-electronics devices.

Research towards developing group III-VI materials as active component in optoelectronics devices has gained a momentum in last couple of years due to their additional advantages over other 2D materials in term of higher carrier mobility, direct band gap electronic structure, high charge density and so on. Particularly, electron mobility of InSe FETs was found to be 1055 $cm^2\ V^{-1}\ s^{-1}$, several magnitude higher than that of TMDs [42]. Hall mobility of InSe was also found to be exceeding $10^3\ cm^2\ V^{-1}\ s^{-1}$ at low temperature [43]. Photoresponsivity of 10^4 A/W and specific detectivity of 10^{13} jones were found in case of InSe photodetectors [44]. InSe photodetector also showed broad spectral response from UV-Visible to near IR [34]. In_2Se_3 phototransistors displays high photo responsivity of 10^5 with specific detectivity reaching ~10^{13}, along with tunable photoresponse by application of back gate [45]. Photoresponsivity of GaTe phototransistor were also found to be ~10^4 A/W [46]. Although photoresponsivity of group III-VI materials is impressive, this devices exhibits slower temporal response. Response time was found to be 8 ms for InSe [44], 40 ms for InSe [34], 9 s for In_2Se_3 [45] and 20 ms for GaTe [46] based photodetectors, which is substantially slower than response time of order of μs in case of MoS_2 [47], WSe_2 [48], and SnS_2 [49] based photodetectors.

Apart from responsivity, response time is another figure of merit of photodetector and it is often regarded as one of the key parameters for developing photodetectors where

functionalities such as fast photo switching are needed. Over past few years, various techniques are being investigated in order to improve electronic and opto-electronic performance of several binary compounds through incorporation or alloying of suitable dopants [50-54]. Most of current research is focused on single elemental, binary systems, their alloys or their heterostructure. It has been shown that elemental composition plays important role in determining physical properties of materials. Multi-elemental systems bring extra degree of freedom via stoichiometric variation. In this respect, ternary systems of Copper Indium Selenide (CIS), in form of thin films and colloidal particles, which has been extensively studied for solar cell applications, may provide new direction to field of electronics.

1.3 Copper Indium Selenide Systems

First CIS photovoltaic device was demonstrated in 1973 at University of Salford where semiconducting crystal of ternary $CuInSe_2$ in indium was used [55]. Most of the subsequent work that followed for developing Cu-In-Se thin films for photovoltaic device application contains $CuInSe_2$ or alloy in multiphase mixture [56]. Bulk Copper Indium Selenide has been widely used in optoelectronics research and industry as a new generation material for ultra-thin flexible solar cell due to its high photoresponsivity and wide spectral range [57].

Ternary CIS comes in various crystal structures depending on ratio between in Copper and Indium [57]. For example, α-CIS has molecular formula $CuInSe_2$, commonly known as chalcopytite and it is characterized by tetrahedral coordination of central atom (can be either cation or anion) with its nearest neighboring atoms. β-phase of CIS is found to be more controversial but simultaneously important for photovoltaic applications. β-CIS comes in different crystallographic structures and it was proposed to have at-least eight different compounds, though $Cu_2In_4Se_7$ and $CuIn_3Se_5$ were dominant. If Copper to Indium ratio lies in-

between 1:5 to 1:9, CIS forms γ-phase and it is found to be in hexagonal stacking of close packed selenium anions, thus yielding layered structure. It is worth noting that among CIS, α-phase is Copper rich where as γ- phase is Indium rich. There exist another phase, δ, which is unstable at room temperature and it usually forms from solidification of ternary liquids or solid phase transformation from either α- or β-phase [57]. Here, we are interested in γ-phase of CIS (Indium rich phases are typically n-type) where it is expected to have layered structure as well as excellent optoelectronics properties of bulk CIS.

Synthesis of 2D CIS has been carried out in the laboratory of Prof. Ajayan at Rice University [58]. They have used chemical vapor transport (CVT) as a route for synthesizing 2D CIS single crystal. CVT has an advantage over other methods as it can control composition of low-volatile compounds. Basic principle of CVT method is introduction (or removal) of one or many components of compound into low-volatile compound at high temperature. According to phase diagram of Cu_2Se-In_2Se_3, at high temperature at-least six different phase coexist depending on the mixture. If percentage of In_2Se_3 lies between 82% and 90%, layered γ- phase dominated. Thus 2D CIS crystal can be synthesized by mixing Cu_2Se and In_2Se_3 in molar ratio of 1:7. This mixture was ground in a mortar to give uniform texture and the resulting mixture is transferred to evacuated quartz ampoule ($<10^{-3}$ torr, flushed with Argon). Further, quartz ampoule was placed in heated furnace at 950^0C for 5 hours. Furnace was slowly cooled down 700^0C at 5^0C/min, followed by naturally cooling to room temperature. As grown CIS crystal has black mica-like texture. Layered CIS has been characterized by SEM, HRTEM, EDX and XRD. The ratio between Copper and Indium has been found to be 1:7 which is consistent with layered phase formation in CIS ($CuIn_7Se_{11}$).

In this thesis, I will discuss various electronic and optoelectronics properties of field effect transistors that were fabricated using few-layers of $CuIn_7Se_{11}$ flakes, which were mechanically exfoliated from bulk crystals. In chapter 2, I will discuss basic characterization of field effect transistor, figures of merits associated with FETs and other key parameters like charge trap density, contact resistance responsible for electronic transport etc. Chapter 3 will focus on improving FET performance by using ionic liquid as top gate instead on SiO_2 back gate and challenges associated with it, mainly estimation of electric double layer capacitance of ionic liquid. Chapter 4 will mainly consist of optical characterization of FET *i.e.* phototransistor, figure of merits associated with phototransistor and key parameter like spectral response and response time essential for developing photodetectors with multiple applications. Some key future directives as well as discussion of the results obtained will be presented in Chapter 5.

CHAPTER 2

FIELD EFFECT TRANSISTOR (FET)

Transistor industry has evolved exponentially during last half century (source: Intel). If Intel's first commercial microprocessor (Intel 4004) is compared with current 14 nm processor, performance has improved by 3,500 times, energy efficiency improved by 90,000 times and cost per transistor is fallen by 60,000 times. To put in perspective, if automotive would have evolved at same rate, cars would go at 300,000 mph with mileage of 2,000,000 mpg and would have cost only $ 0.04 [59]. Certainly no other technology has progressed at this rate and had an impact on society throughout the world.

In 1965, Intel co-founder Gordon Moore has predicted that number of transistor in integrated circuit would double every two years. Intel 4004 contained approx. 2300 transistors on microprocessor chip, whereas current core i7 processor contains almost 2 billion transistor in same size microprocessor chip (source: Intel). That is similar asking entire population china to fit into average size music hall. This scaling was possible due to evolution of transistor technology like integration of metal-oxide-semiconductor field-effect transistor (MOSFET) into microprocessor in 1970s, incorporation of strained Silicon in early 2000s and inclusion high κ metal gate and tri-gate (FinFET) in 2010s (source: Intel). It is worth noting that technology has evolved in two main direction: device architecture and materials system. In terms of device architecture, we are focused on developing electric double later field effect transistor (EDL-FET), (discussed in chapter 3).

As discussed before, 2D materials are regarded as future candidates for electronics industry and ternary system of $CuIn_7Se_{11}$ may give new direction to field of electronics. Here I will demonstrate 2D $CuIn_7Se_{11}$ flakes for field effect transistor. Before going into experimental

section, I would like to discuss some basic features and figure of merits of FETs.

2.1 Introduction to FET

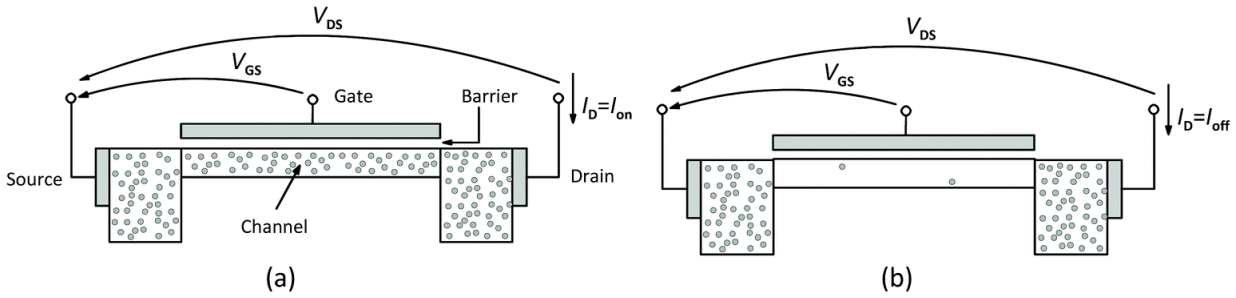

Figure 2.1: General FET Structure in a) on-state and b) off-state. Reproduced from Ref. [60] with permission from the Royal Society of Chemistry.

A basic structure of FET is shown in figure 2.1. A FET consists of a region called the channel, which connects two charge reservoirs, known as the source and the drain. A third electrode, known as gate, is separated from channel by isolator (usually insulating metal oxide). An applied drain-source voltage (V_d) drives a drain current (I_d) through channel and applied gate-source voltage (V_g) controls I_d by controlling conductivity of channel. FETs are commonly utilized as on\off switch and as a signal amplifier. FET is in on-state when channel has high conductance (low resistance) and large I_d, as shown in figure 2.1a. Typically on-current, I_{on} is defined as maximum drain current flowing through a channel when it is in on-state. FET is in off-state when channel has low conductance (high resistance) and only small I_d is allowed to flow, as shown in figure 2.1b. Off-current I_{off} is defined as current flowing through channel when it is in off-state. Gate voltage at which transistor is on verge of switching on is known as threshold voltage (V_{th}).

A transfer characteristics of FET is a response of drain current, I_d with by varying gate voltage, V_g at constant drain voltage V_d. A typical transfer characteristics of FET is shown in figure 2.2. Subthreshold region of transfer characteristics is defined as region when drain current,

I_d depends exponentially on gate voltage V_g, and it occurs when ($V_g < V_{th}$). Subthreshold region is followed by transition region around V_{th} and finally by superthreshold region. Superthreshold region of transfer characteristics is defined as region when drain current, I_d depends linearly on gate voltage V_g, and it occurs when ($V_g > V_{th}$).

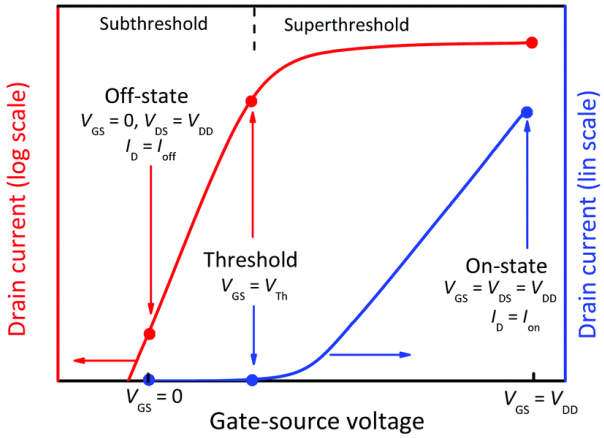

Figure 2.2: A typical transfer characteristics of FET. Reproduced from Ref. [60] with permission from the Royal Society of Chemistry.

A figure of merit associated with switching is on-off ratio. As name suggests, on-off ratio is defined as ratio of on-current to off-current (I_{on}/I_{off}). Ideal on-off ratio for FET is considered to be 10^4-10^7. As a basic rule, off-current should be as low as possible in order for low power consumption at off-state of FET [60]. [Note: Remember, currently a microprocessor IC has almost 2 billion transistor and if I_{off} of FET is 1 nA, off-state current for IC would be ~ 2 A.]

Another figure of merit for evaluating FET performance is known as field-effect mobility (μ_{FE}). In simple words, mobility is defined as average drift speed of charge carriers under unit electric field, thus high mobility means more carries are passing through channel per unit time. High mobility is essential for higher screen luminance and resolution, decrease power dissipation, increase switch speed and achieve high speed [61]. According to gradual channel approximation, drain current, I_d of FET can written as shown in Eq. 2.1.

$$I_d = \frac{W}{L}\,\mu_{FE}\,C_g\left[\left(V_g - V_{th}\right)V_d - \frac{V_d^2}{2}\right] \quad \text{.....Eq. 2.1}$$

Where, μ_{FE}, V_g, V_{th} and V_d are quantities defined above, C_g is capacitance of gate dielectrics per unit area, and W and L are channel width and length respectively. In superthreshold region of transfer characteristics (when $V_d << V_g - V_{th}$), Eq. 2.1 can be simplified as to Eq. 2.2.

$$I_d = \frac{W}{L}\,\mu_{FE}\,C_g\,V_d\left(V_g - V_{th}\right) \quad \text{.....Eq. 2.2}$$

The field effect mobility can be obtained at low V_d by Eq. 2.3,

$$\mu_{FE} = \frac{L}{W\,C_g\,V_d}\,\frac{\partial I_d}{\partial V_g} \quad \text{.....Eq. 2.3}$$

where slope ($\partial I_d/\partial V_g$) is taken at linear region of transfer curve.

Subthreshold swing (SS) is consider as another figure of merit and it reflects gate voltage, V_g, required for increasing drain current, I_d, by an order of magnitude in subthreshold region. SS is determined by inverse of maximum slope of transfer curve, as shown in Eq. 2.4.

$$SS = \left(\left|\frac{\partial \log(I_d)}{\partial V_g}\right|_{max}\right)^{-1} \quad \text{.....Eq. 2.4}$$

Subthreshold swing of a FET device can also be given by Eq. 2.5 [62],

$$SS = \ln(10)\,\frac{k\,T}{e}\left(1 + \frac{C_d}{C_{ox}}\right) \quad \text{.....Eq. 2.5}$$

where, e is electronic charge, k is Boltzmann constant, T is temperature, C_d is depletion layer capacitance and C_{ox} is oxide capacitance. A minimum limit of SS can be found by letting $C_d/C_{ox} \rightarrow 0$, physically it means effect of depletion layer (mostly formed by either p-n junction or trap charges) is negligible compared to oxide capacitance. At room temperature (300 K), minimum achievable SS is ~ 60 mV/dec by substituting $C_d/C_{ox} \rightarrow 0$ in Eq. 2.5.

2.2 Experimental Section

The bulk crystals of layered $CuIn_7Se_{11}$ were grown using chemical vapor transport technique by our collaborator at Rice University [58]. Few layers of $CuIn_7Se_{11}$ were exfoliated using scotch tape assisted mechanical exfoliation on SiO_2/Si substrate with 300 nm of oxide layer. Insulating SiO_2 will be used as gate for FET characterization and commonly known as back gate. Chromium (Cr) and Gold (Au) metals were used for making contacts. Metal contact of Cr (~20 nm) and Au (~240 nm) were deposited on as-exfoliated flakes of $CuIn_7Se_{11}$ by using a house built thermal evaporation system through a metal shadow mask. Atomic-force microscopy (AFM) was performed in order to determine number of layers. From AFM height profile, it was concluded that thickness of $CuIn_7Se_{11}$ flake is about ~ 66 nm which correspond to roughly 40 layers (as each layer is 1.6 nm thick). After metal contact deposition, SiO_2 wafer was transferred onto chip holder (Spectrum Semiconductor, CSB02842) and glued using silver paste. Cr/Au contacts were connected with chip holder by wire bonding using Au wire.

In order to study electronic transport, as-connected chip holder was mounted on the cold head of the cryostat (SHI Cryogenics Group, RDK-101D) and Keithley 24xx-series Source Meters were used to source and measure voltage and/or current at source, drain and gate terminal of FETs, through BNC cables. Keithley SourceMeters were controlled through LabVIEW 2015 (National Instruments) via General Purpose Interface Bus, GPIB (IEEE 488 interface). Collected data was plotted and analyzed using OriginPro 2015. All experiment were carried out under high vacuum in order to nullify effect of adsorbed molecule and high vacuum (~ 10^{-5} torr) is achieved through mechanical and turbo pump (BOC Edwards).

2.3 Results and Discussions

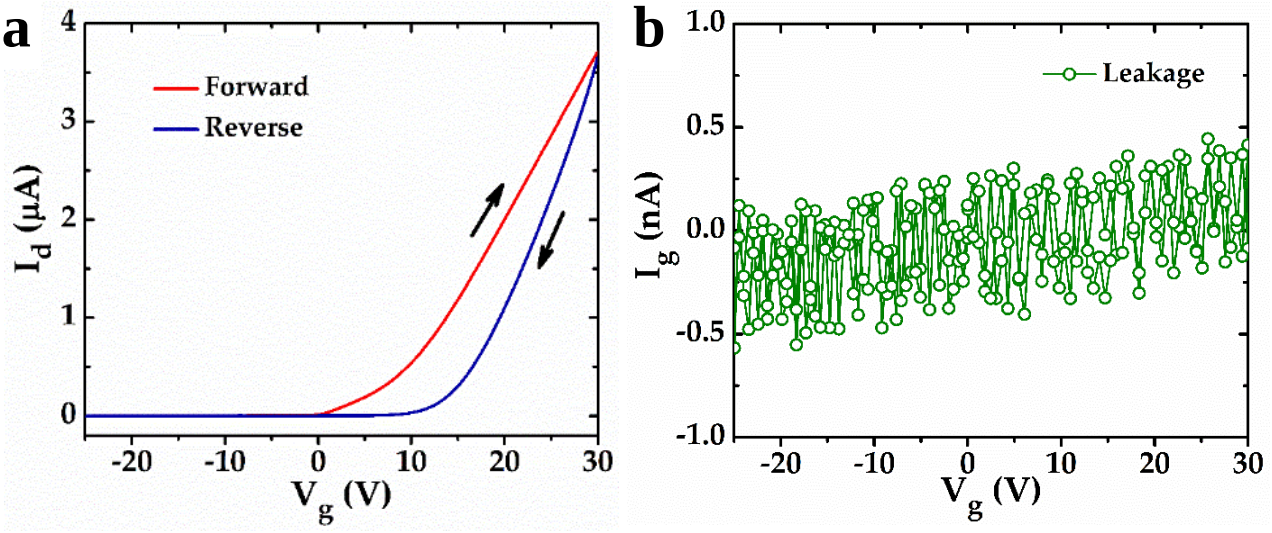

Figure 2.3: a) A transfer characteristics of $CuIn_7Se_{11}$ FET for forward cycle (blue), reverse cycle (red). b) SiO_2 back gate leakage current as a function of applied gate voltage.

Electronic transport measurements of $CuIn_7Se_{11}$ FET using SiO_2 as back gate is shown figure 2.3 and 2.4. Figure 2.3a shows transfer characteristics between gate voltage of -25 V to +30 V and at constant drain voltage of 0.2 V. A typical n-type semiconducting behavior is observed which is reasoned to In-rich nature of CIS system. Here I would like to mention that hysteresis is observed with cycling of back gate voltage, which is indication of charge trapping at $CuIn_7Se_{11}$ and SiO_2 interface (detailed explanation is given later in chapter). We have used forward cycle (gate voltage sweep from -25 V to +30 V) in order to calculate figures of merits associated with FET. A maximum drain current of 3.6 μA was observed in on-state of FET and drain current of 100-300 pA was observed in off-state of FET. It is to be noted that gate leakage current was limited to 500 pA (at highest applied gate voltage of +30 V), as shown in figure 2.3b and it is 4 order of magnitude less than on-state current. It is desired to have low gate leakage current in order to minimize operating energy consumption.

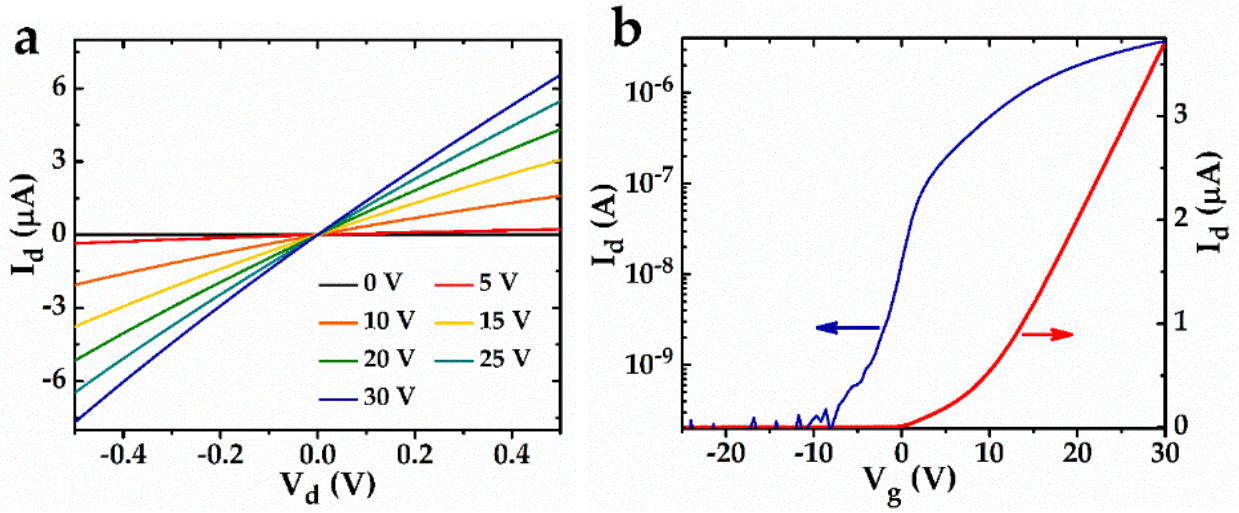

Figure 2.4: a) Output characteristics under different gate bias conditions (0 V ≤ V_g ≤ + 30 V) are shown. b) A transfer characteristics of $CuIn_7Se_{11}$ FET for forward cycle.

Output characteristics of FET determines properties of metal-semiconductor junction at contacts. Fermi levels at metal-semiconductor junction can either match or mismatch. Fermi level mismatch which leads to formation of barrier, known as Schottky barrier and contact is known as Schottky contact. Schottky contacts are rectifying in nature, meaning contacts provides high resistance for flow of electron from metal to semiconductor or vice versa. Fermi levels matching leads to ohmic contact and usually ohmic contact are non-rectifying contacts (low resistance), which allows flows of electron from metal to semiconductor or vice versa. Thus ohmic contacts are desirable for good performance of FETs. However formation of Schottky barrier within material is essential in other types of semiconducting devices like Schottky diode, bi-polar junction transistors etc. One of the properties of ohmic contact is linear current voltage (I-V) curve, which follows ohm's law. Output characteristics of FET is response of drain current, I_d, caused by variation of drain voltage, V_d. Output characteristics of $CuIn_7Se_{11}$ FET under different gate bias condition (0 V ≤ V_g ≤ +30 V) is shown in figure 2.4a. An almost linear behavior of I_d-V_d curves within applied voltage region where measurements are performed,

indicates that contacts are 'ohmic-like contacts' and barrier effects can be neglected.

2.3.1 Figure of merits: mobility, subthreshold swing, on/off ratio

We have used forward cycle of transfer curve to estimated figure of merits and it is shown in figure 2.4b. A threshold voltage was found to be ~ 8.1 V by extrapolating linear portion of superthreshold region. Field effect mobility was calculated from linear region of transfer curve (superthreshold region) using Eq. 2.3. Device under investigation has the channel length, L, of ~ 10 μm and the channel width, W, of ~ 20 μm. The oxide capacitance (C_{ox} = 1.16 * 10^{-8} F) is calculated by using formula, $C_{ox} = \varepsilon_0 \varepsilon_r / d_{ox}$, where, ε_r = 3.9 and d_{ox} = 300 nm are the relative permittivity and thickness of the SiO_2 layer respectively. A constant drain voltage (V_d) of 0.2 V is applied throughout measurement. A transconductance, g_m, defined as change in drain current, I_d, divided by change in gate voltage, V_g, at constant drain voltage, V_d, *i.e.* $g_m = \partial I_d / \partial V_g$. For device under investigation, transconductance, g_m, of ~ 1.7 * 10^{-7} S were estimated. Usually, transconductance is normalized by channel length, 10 μm. Thus normalized transconductance g_m is 17 mS/μm and it is a two order higher than that of FinFET (g_m = 0.6 mS/μm) [63], which is current technology used for semiconductor device fabrication (also known as 14 nm node) by Intel and other leading manufactures. The room temperature field effect electron mobility of $CuIn_7Se_{11}$ FET was estimated to be μ_{FE} ~ 36.89 $cm^2 V^{-1} s^{-1}$ which is significantly higher or comparable with electron mobility of In_2Se_3 (μ_{FE} ~ 30 $cm^2 V^{-1} s^{-1}$) [45], In_2Se_3 (μ_{FE} ~ 2.5 $cm^2 V^{-1} s^{-1}$) [38], InSe (μ_{FE} ~ 0.1 $cm^2 V^{-1} s^{-1}$) [34], InSe (μ_{FE} ~ 32.6 $cm^2 V^{-1} s^{-1}$) [44], GaTe (μ_{FE} ~ 0.2 $cm^2 V^{-1} s^{-1}$) [46], and GaSe (μ_{FE} ~ 0.1 $cm^2 V^{-1} s^{-1}$) [64] based FETs.

Our measurements shows on-state current, I_{on} ~ 3.6 * 10^{-6} A and off-state current, I_{off} ~ 3 * 10^{-10} A. Thus on-off ratio was found to ~10^4, which lies in range of ideal on-off ratio. To calculate subthreshold swing, transfer curve is plotted in logarithmic scale (log with base 10) in

figure 2.4b (blue curve) and slope ($\partial \log(I_d)/ \partial V_g$) of curve was calculated in subthreshold region. Subthreshold slope was found to 0.41 dec/V which correspond to subthreshold swing, SS of 2.44 V/dev. 22 nm tri-gate transistor used in CMOS technology has SS of ~ 70 mV/dec [65], which is close to ideal SS (~ 60mV/dec). As mentioned earlier, deviation of SS from ideal SS can be attributed to presence of trap charges, which try to counter oxide gate effect.

2.3.2 Trap density calculation

As mentioned earlier, trapping of charge has direct consequence on electronic transport. For example, observation of hysteresis in with cycling of applied back gate voltage and deviation of SS from ideal. Thus it is important to know estimated charge trap density. In a typical semiconductor, traps state can be classified into two types, bulk traps states and interface trap states. Bulk traps states are mid-gap states present in-between band gap of semiconductor and arises due to various defects present in crystals. Interface trap states comes from states present at interface between semiconductor and substrate underneath. Interface traps states plays crucial roles in nano-structured semiconductor due to low surface to volume ratio.

Under assumption of density of trap states (both bulk and interface) are independent of energy, Eq. 2.5 can be simplified as follows, Eq. 2.6 [66],

$$SS = \ln(10)\ \frac{k\,T}{e}\ \left(1 + \frac{e^2\ N_{tr}}{C_{ox}}\right) \quad \text{.....Eq. 2.6}$$

where N_{tr} is trap density of states, DOS (per unit area and unit energy). At room temperature, using SS = 2.44 V/dec and C_{ox} = 1.16 * 10^{-8} F, trap DOS can estimated to be, N_{tr} = 3.1 * 10^{12} cm^{-2} eV^{-1}. Estimated trap DOS are comparable with other 2D based FET devices [67-69].

Hysteresis observed in transfer characteristics is common indication of charge trapping at $CuIn_7Se_{11}$ and SiO_2 interface. Thus, interface trap density ($n_{tr/intf}$) can be estimated by change in threshold voltage (ΔV_{th}) by equation $n_{tr/intf} = C_{ox}\ \Delta V_{th}/e$ [45]. Here, we observed threshold

voltage for forward cycle to be $V_{th/for} \approx 8.1$ V and threshold voltage for reserve cycle to be $V_{th/rev} \approx 16.4$ V. Thus change in threshold voltage, $\Delta V_{th} \approx 8.3$ V, which correspond to interface trap density, $n_{tr/intf} \approx 5.97 * 10^{11}$ cm^{-2}. Note that $n_{tr/intf}$ is number density and correspond to actual number of trap state present.

2.3.3 Estimation of contact resistance

As mentioned earlier, contact resistance plays important role in electronic transport. Contacts for $CuIn_7Se_{11}$ FET indicates 'ohmic-like contacts'. Contact resistance and other electrical characteristics can be estimated by Y-function method [70], which was proposed by Ghibaudo [71].

Y-function method is based on analysis of drain current in superthreshold region *i.e.* linear region of transfer characteristics. Considering addition voltage drop at source and drain due to contact resistance (R_c), Eq. 2.1 can be re-written by Eq. 2.7 [72],

$$I_d = \left(\frac{\mu_0}{1 + \theta_0 \left(V_g - V_{th}\right)}\right) \frac{W}{L} C_g \left(V_g - V_{th} - 0.5\, V_d\right) \left(V_d - I_d\, R_c\right) \quad \text{.....Eq. 2.7}$$

where, θ_0 is first-order mobility attenuation coefficient, and it is introduced to depict the realistic device performance by taking into account of remote phonon scattering and surface roughness and μ_0 represent low-field mobility. At low-electric field, drift velocity is proportional to the electric field, thus mobility, μ is constant. Under low-field bias condition $V_g - V_{th} >> 0.5V_d$ in superthreshold region, $0.5V_d$ factor can be neglected. For convenience of calculation, θ_0 and R_c factor can be combined as one effective attenuation factor, θ as $\theta = \theta_0 + \mu_0.R_c.C_g.W/L$. Thus Eq. 2.7 can be re-written as Eq. 2.8

$$I_d = \left(\frac{\mu_0}{1 + \theta \left(V_g - V_{th}\right)}\right) \frac{W}{L} C_g \left(V_g - V_{th}\right) V_d \quad \text{.....Eq. 2.8}$$

Y-function is defined as $I_d/\sqrt{g_m}$, where $g_m = \partial I_d/\partial V_g$ is transconductance. Here we assume

that contact resistance, R_c does not depend on gate voltage, V_g, since Schottky barrier at contact is negligible. Thus in this case, Y-function is given by Eq. 2.9.

$$Y = \frac{I_d}{\sqrt{g_m}} = \sqrt{\frac{\mu_0 \, C_g \, V_d \, W}{L}} \left(V_g - V_{th}\right) \quad \text{.....Eq. 2.9}$$

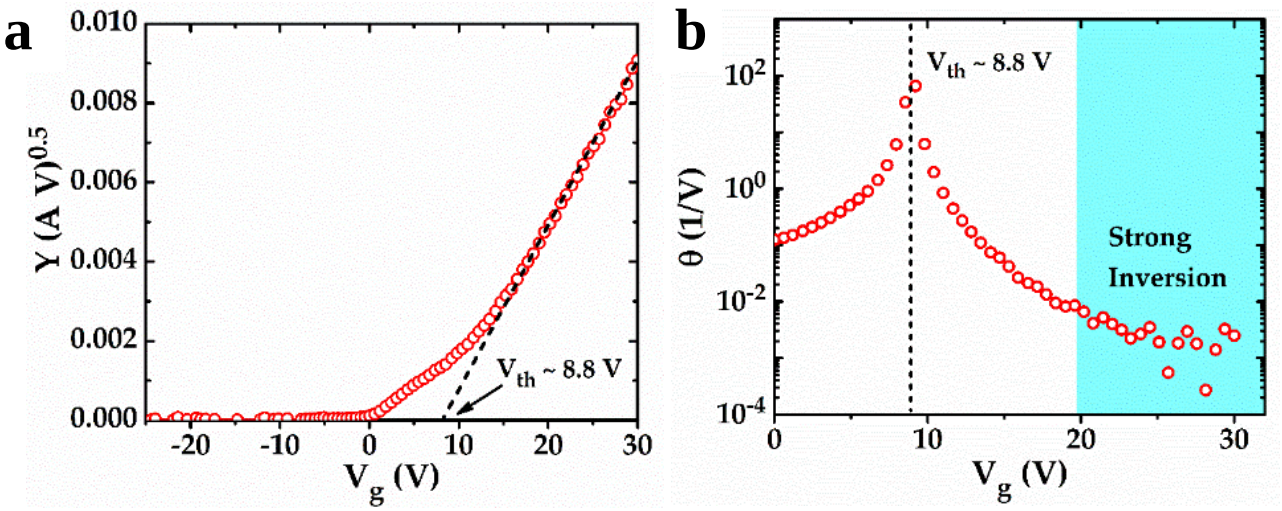

Figure 2.5: Y-function analysis of $CuIn_7Se_{11}$ FET a) Y-function as a function of gate voltage b) effective attenuation factor as function of gate voltage.

Figure 2.5 represent extraction of various electrics characteristics by simplified Y-function method. Variation of Y-function with respect to gate voltage is shown in Figure 2.5a. From linear fit in strong inversion region (or superthreshold region), threshold voltage, $V_{th} \approx 8.8$ V can be extracted from x-intercept and low-field mobility, $\mu_0 \approx 39.91$ $cm^2 V^{-1} s^{-1}$ can be extracted from slope. It has to be noted that threshold voltage calculated by Y-function method is more accurate that threshold voltage estimated earlier and both methods gives close values (within 10% error). Also, we have estimated that field-effect mobility, $\mu_{FE} \approx 36.89$ $cm^2 V^{-1} s^{-1}$ which is significantly lower that low-field mobility. It is to be noted that, in presence of contact resistance, extracted field-effect mobility can be significantly underestimated than its true low-field mobility. Relation between mobilities and resistance can be given by following equation

Eq. 2.10, [70]

$$\frac{\mu_{FE} - \mu_0}{\mu_0} = \left(\frac{R_c}{R_{tot}}\right)\left(\frac{R_c}{R_{tot}} - 2\right) \quad \text{.....Eq. 2.10}$$

Where, R_{tot} is total resistance of device (channel plus contact). However, μ_{FE} is very close to μ_0 and it can be deduced that $R_c << R_{tot}$, *i.e.* contact resistance is negligible.

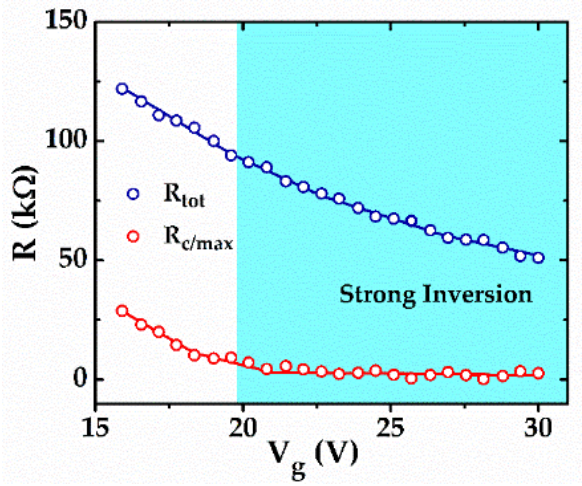

Figure 2.6: Comparison of upper limit of contact resistance and total resistance of device (channel plus contact).

In order to further estimate contact resistance quantitatively, effective attenuation factor, θ is plotted as function of gate voltage, V_g in figure 2.5b. In limit of negligible first order mobility attenuation coefficient, θ_0, an upper bound can be placed on contact resistance through equation $\theta \approx \mu_0.R_c.C_{ox}.W/L$. In strong inversion region, contact resistance is extracted to be $R_{c/max} \approx 2.8$ kΩ. A comparison of total resistance and contact resistance is shown in figure 2.6 and in strong inversion region, $R_{tot} > 50$ kΩ whereas $R_{c/max} \approx 2.8$ kΩ. Thus it can be concluded that contact resistance will not play a crucial role in governing electronic properties of $CuIn_7Se_{11}$ FET.

2.4 Conclusion

In conclusion, field effect transistor is fabricated using few layers of layered $CuIn_7Se_{11}$

flakes which were mechanically exfoliated from single crystals grown using chemical vapor transport technique. Our FET characterization shows, ohmic-like contacts, field-effect mobility, μ_{FE} of 36.89 $cm^2\ V^{-1}\ s^{-1}$, on-off ratio of ~10^4, and subthreshold swing, SS of 2.44 V/dev. It was inferred that deviation of SS from ideal SS is due presence of charge trap states at bulk and interface and trap density of states (DOS) was estimated to be $N_{tr} = 3.1 * 10^{12}\ cm^{-2}\ eV^{-1}$. Our Y-function analysis shows contact resistance is negligible compared to total resistance of device, threshold voltage, V_{th}, of ~ 8.9 V, and low-field mobility, μ_0, was estimated to be 39.91 $cm^2\ V^{-1}\ s^{-1}$. Similar devices were used to study the effect of electrolyte (top) gating also referred as electric double layer (EDL) – FET. Optical properties of SiO_2 back gated FETs, known as phototransistors were also measured. The results of these measurements are presented in chapter 3 and chapter 4, respectively.

CHAPTER 3

ELECTRIC DOUBLE LAYER (EDL) - FET

One of the reason transistor industry was able to cope with Moore's law is evolution in transistor device architect. As mentions before, integration of metal-oxide-semiconductor field-effect transistor (MOSFET) into microprocessor in 1970s, incorporation of strained Silicon in early 2000s and inclusion high κ metal gate and tri-gate (FinFET) in 2010s are few examples of evolution in transistor (source: Intel).

In FETs, conductivity of channel is controlled by gate terminal through applied gate-source voltage (V_g). The gate is separated by semiconductor channel by insulator which act-like dielectric medium. Traditionally silicon (Si) was used as semiconductor channel and silicon dioxide (SiO_2) was used as gate terminal which are core components of FETs. SiO_2 is most commonly used gate dielectric as it can be fabricated easily and etched into various size using thermal oxidation of silicon. However it is shown in recently that organic compounds, polymers, nanocomposites and/or complex oxides can be used as gate dielectrics depending on cost, durability, operation speed and transconductance [73,74]. Also, FET characteristics can be greatly affected by properties of dielectric-semiconductor interface. Most important figure of merits for potential gate dielectric is specific capacitance as it determines charge carrier density that can be induced in channel of FET.

As it can be seen from Eq. 2.1 that capacitance of gate dielectric, C_g is directly proportional to drain current, I_d and inversely proportional to threshold voltage, V_{th}. Also, in case of parallel plate capacitor, charge accumulated at surface of plate, Q can be written in terms of parallel plate capacitor, C and applied voltage, V as Q = C * V. Thus, it can be deduced that high capacitance can yield in high charge carrier density which give rise to high on-state current and

low threshold / operational voltage.

The capacitance of a parallel plate capacitor can be given by Eq. 3.1, as follows

$$C = \frac{\varepsilon_0 \, \varepsilon_r \, A}{d} \quad \text{.....Eq. 3.1}$$

where, ε_0 is vacuum permittivity ($\varepsilon_0 = 8.85 * 10^{-12}$ F m^{-1}), ε_r is relative permittivity of dielectric material with respect to vacuum, A is area of plate, and d is distance between two plates. For, SiO_2 gate dielectric ($\varepsilon_r = 3.9$) of thickness d = 300 nm, an oxide capacitance, C_{ox} of $1.16 * 10^{-8}$ F can be estimated. Note that it is possible to estimate capacitance of SiO_2 dielectric assuming that it behaves as parallel plate capacitor. With 300 nm thick SiO_2 dielectric, typical charge carrier density of ~ 10^{13} cm^{-2} can be attainted. Although this value of charge carrier density is sufficient for modulating conductivity in semiconductor, it is incapable of inducing drastic changes in electronic properties like superconductivity and ferroelectricity. One can argue that applied voltage can be increased to induce more charges but it has to be noted that dielectrics breakdown at large voltages, known as dielectric breakdown.

According to Eq. 3.1, gate capacitance, C_g, can be increased by either by using dielectric with higher relative permittivity, ε_r, or increasing area of dielectric, A, or by reducing thickness of dielectric, d. Note that there are limited number of dielectric available to use. TiO_2 tend to have highest relative permittivity of $\varepsilon_r = 41$ [75], which corresponds to approximately an order of magnitude increase in gate capacitance. Another option is to increase area of dielectric. It would not be a feasible option as it will correspondingly increases area of channel which will affect scaling of transistor and lower current flowing through channel (higher resistance). Last option is to decrease thickness. As thickness of dielectric is reduced, dielectric breakdown voltage is lowered, increase gate leakage current and stability of gate will be compromised.

3.1 Introduction to EDL-FET

Capacitors are conventionally used as energy storage system in which charges are stored on plates of parallel plate capacitor. In past few years, electric double layer capacitor, EDLC, has emerged where charges are stored at interface of solid and electrolyte. In EDLC, higher surface area can be achieved through porosity of nanostructure and charges are separated by interface thus giving atomically thick capacitor. Thus capacitance of EDLC is several order of magnitude higher than that of conventional parallel plate capacitor, which can be seen by Eq 3.1.

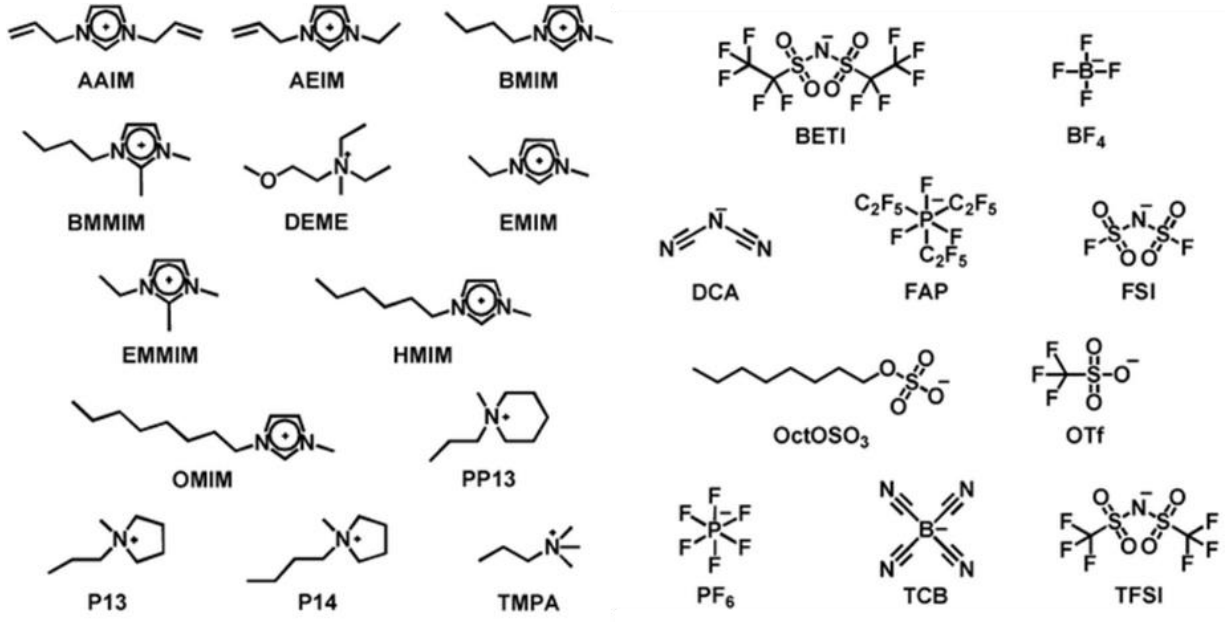

Figure 3.1: Molecular structures and abbreviations of cations and anions of ionic liquid. Reproduced from Ref. [89] with permission from the Royal Society of Chemistry.

In past couple of years, ionic liquids have attracted attention over organic solvents and aqueous solution due to their stability and non-volatile nature. Ionic liquids are binary salts that are composed purely of ions, organic cation and inorganic anions. Some of the example of anions are shown in figure 3.1. Ionic liquids have various advantages such as they does not exhibits solvation effect, displays high thermal stability *i.e.* exist in fluid state over wide temperature, high electro-chemical stability *i.e.* wide electrochemical windows (no redox

reaction when exposed to high potential), highly polarizability *i.e.* separation of cation and anion, low melting point, non-volatility *i.e.* maintained at constant concentration and nontoxicity etc. Due to this properties, ionic liquids can be regarded as potential candidate for gate dielectric material in FETs.

Although devices with EDL were proposed in 1970 [76], a significant breakthrough was made in 2007 a group from Germany demonstrated electric field induced modification in magnetism by forming EDL at interface of electrolyte (propylene carbonate) and epitaxial films of FePt or FePd [77]. Since then various groups have carried out large amount of research towards incorporating EDL in various devices. For examples, shift in Dirac point was observed in graphene FET with change in concentration of ionic liquid thus it can be used as biosensor [78], a superconductivity was induced in atomically flat film of layered nitride compound of ZrNCl at T = 15.2 K by using ionic liquid DEME-TFSI [79], electric field induce transition from insulating state to metallic state in thin flakes of Black Phosphorus which shows ambipolar transport in FET when gated with ionic liquid [80], ferromagnetism can be induced electrostatically in cobalt (Co) doped titanium dioxide (TiO_2) in EDL-FET structure [81], and lastly device performance was shown to improve in case of few layered MoS_2 ambipolar FET with mobility increasing to ~ 60 $cm^2 V^{-1} s^{-1}$, on-off ratio improved to ~ 10^7 and subthreshold swing reaching near ideal value of ≈ 50 mV/dec [82].

Although EDL shows extraordinary properties, practically it is very difficult to carry out experiments because of viscous nature of ionic liquids. Researchers have used polymer gel matrix to support ionic liquids [83] but there is plenty of room for improvement. Another shortcoming of using EDL in FET is estimation of electric double layer capacitance as it depends on electrolyte-semiconductor interface [61]. For example, DEME-TFSI is widely used as

electrolyte for EDL-FETs and electric double layer capacitance, C_{EDL}, was found to vary as C_{EDL} ≈ 9.2 μF cm^{-2} for ZrNCl [79], C_{EDL} ≈ 7.2 μF cm^{-2} (electron) and ≈ 4.7 μF cm^{-2} (hole) for MoS_2 [84], C_{EDL} ≈ 34 μF cm^{-2} for ZnO [85], and C_{EDL} ≈ 20 μF cm^{-2} for VO_2 [86]. Thus it is utmost important to estimated actual EDL capacitance at electrolyte-semiconductor interface in order to accurately quantify performance of EDL-FET.

Several techniques have been used in order to estimate EDL capacitance. For example, electrochemical impedance spectroscopy (EIS) was used to evaluate EDL capacitance in ZnO thin film transistor [87], Hall effect measurement was used to estimated EDL capacitance in MoS2 thin flake transistors [84], interconnection between SiO_2 back gate and ionic liquid top gate, in particular change in threshold voltage, V_{th}, with application of back gate voltage in dual gating FET [82], and Mott-Schottky analysis was used for organometal perovskite solar cells to extract depletion layer capacitance at interface [88]. Here we have used Mott-Schottky analysis to extract capacitance of $CuIn_7Se_{11}$ based EDL-FET using ionic liquid electrolyte [1-Butyl-3-methylimidazolium hexafluorophosphate (BMIM-PF_6)].

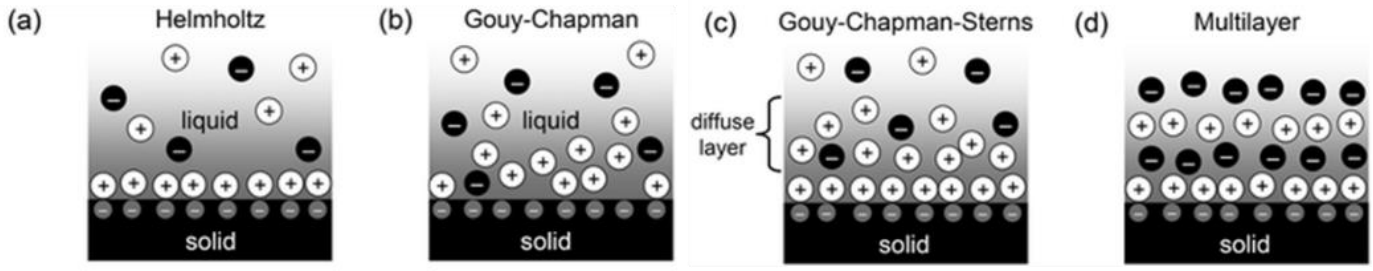

Figure 3.2: Models describing electrolyte-semiconductor interface. a) Helmholtz model, b) Gouy-Chapman model, c) Gouy-Chapman-Sterns model, and d) multilayer model. Reproduced from Ref. [89] with permission from the Royal Society of Chemistry.

Before going into detailed study of EDL-FET, it is crucial to understand how EDL are formed. Various models have been proposed in order to explain how ionic liquid behaves at

electrolyte-semiconductor interface and shown in figure 3.2. The Helmholtz model [89,90] considers EDL formed by a single ion layer in solution which is adsorbed on solid surface, as shown in figure 3.2a. Thus, in Helmholtz model, mathematically EDL can be treated as parallel plate capacitor formed by ions in electrolyte and charges in semiconductor, separated by solid-liquid interface. Gouy-Chapman model [91,92] takes diffusion property of ionic liquid into account, which basically states that electrical potential decays exponentially with distance from solid-liquid interface, as shown in figure 3.2b. Though this model does not work for highly polarizable EDLs. Gouy-Chapman-Stern model [93] combines Helmholtz model (internal Stern layer) and Gouy-Chapman model (outer diffuse layer), as shown in figure 3.2c. However this model was developed for dilute solutions where solute ions are well separated. For molten salts, multilayer model was proposed [94,95] which considers polarization of ionic charges in multilayer structures, as shown in figure 3.2d. We have used 1-Butyl-3-methylimidazolium hexafluorophosphate (BMIM-PF_6) as ionic liquid for $CuIn_7Se_{11}$ based EDL-FET and it was shown that ions of BMIM-PF_6 forms Helmholtz-like layer with potential drop occurs within ~ 3 Å of solid surface [96].

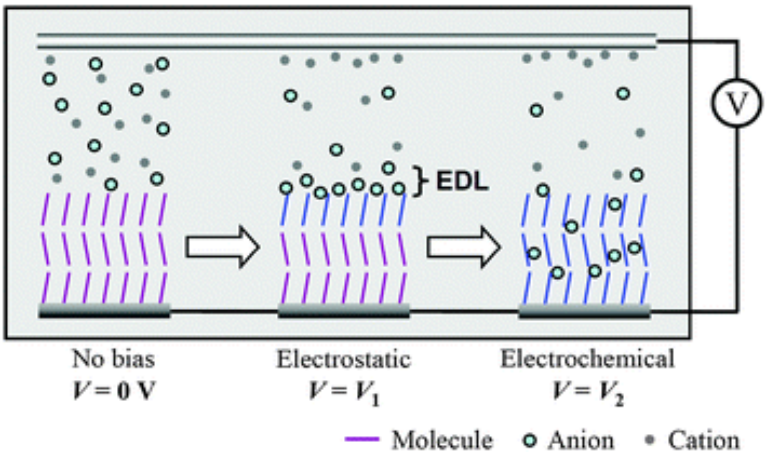

Figure 3.3: Electrostatic and electrochemical interaction at electrolyte-semiconductor interface. Reproduced from Ref. [89] with permission from the Royal Society of Chemistry.

While operation with EDL-FET, attention has to be given towards applying voltage. figure 3.3 shows electrostatic and electrochemical model of electrolyte-semiconductor interface [97]. For zero bias voltage (V = 0 V), there is no/minimal interaction between ions and semiconductor. For a voltage $V_1 > 0$ V (or < 0 V), anions (or cations) accumulate at the interface, forming EDL. For higher voltages, $|V_2| > |V_1|$, electrochemical reaction takes place and most of cases it is irreversible process which results in degradation of transistor performance. However EDL-FET have various advantages over dielectric based FETs. In EDL, potential drops are restricted to size of ions (layer formation) which is contrary to solid state dielectric material where potentials changes linearly, shown in figure 3.4. Thus, EDL generates high local electric field which operate EDL-FETs at low voltage and allows high charge carrier accumulation.

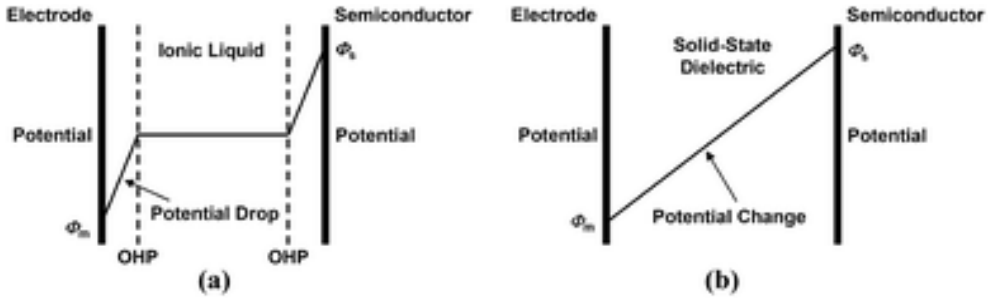

Figure 3.4: Variation of potential inside the dielectric materials in case of a) ionic liquid and b) solid state dielectric. Reproduced from Ref. [89] with permission from the Royal Society of Chemistry.

3.2 Experimental Section

Experimental methods for EDL-FETs is exact same as that of FET (mentioned previously in chapter 2). Only dissimilarity is that, here we have used 4 terminals. Two terminals are source and drain, which are connected to $CuIn_7Se_{11}$ channel. Third terminal was connected to Si, which was separated by SiO_2 from $CuIn_7Se_{11}$ channel, thus using SiO_2 as back gate terminal. Fourth terminal is used to control EDL formed by BMIM-PF_6 ionic liquid. We have used gold pad which is close $CuIn_7Se_{11}$ channel, to make a connection with Keithley 24xx-series SourceMeter.

A small and continuous drop of IL, BMIM-PF_6 was placed such a way that it is in contact with $CuIn_7Se_{11}$ channel and gold pad with minimal area coated. Performance of EDL-FET was evaluated by investigating transfer and output characteristics. BMIM-PF_6 ionic liquid were purchased from ACROS Organics, a Thermo Fisher Scientific brand (CAS No.: 174501-64-5) and used directly in experiments without further treatment.

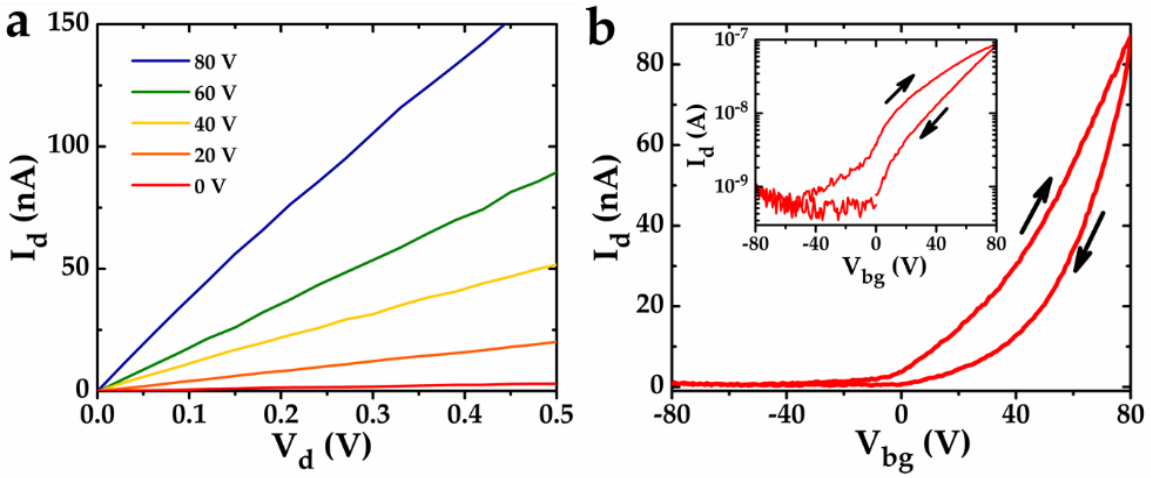

Figure 3.5: a) Output characteristics under different back gate bias conditions (0 V ≤ V_{bg} ≤ + 80 V) are shown. b) A transfer characteristics of $CuIn_7Se_{11}$ FET for forward cycle and reverse cycle using back gate. Inset: Transfer characteristics in log scale for drain current.

3.3 Results and Discussions

FET was fabricated and analyzed as discussed in chapter 2. Briefly, few layers of $CuIn_7Se_{11}$ mechanically exfoliated using scotch tape on 1000 nm of thick SiO_2/Si substrate. Metal contact consist of Cr and Au were deposited using thermal deposition by shadow mask technique. The oxide capacitance (C_{ox} = 3.45 * 10^{-9} F cm^{-2}) was calculated by using formula, $C_{ox} = \varepsilon_0 \varepsilon_r / d_{ox}$, where, ε_r = 3.9 and d_{ox} = 1000 nm are the relative permittivity and thickness of the SiO_2 layer respectively. Transfer and output characteristics of $CuIn_7Se_{11}$ FET is shown in figure 3.5. Output characteristic shows 'ohmic-like' contacts within measured voltage bias. Transfer characteristics shows typical n-type electrical transport with estimated figures of merits are field-

effect mobility, $\mu_{FE} \approx 2.66\ cm^2\ V^{-1}\ s^{-1}$, on-off ratio ~$10^2$, and subthreshold swing, SS ≈ 29.8 V/dev. Hysteresis was observed while cycling with back gate voltage indicating charge trap states present at $CuIn_7Se_{11}$ and SiO_2 interface. Performance of device used for EDL-FET is poor compared to other devices measured and it might be caused either due to thicker SiO_2 layer used for this device or other factors like deposition of metal contacts, number of $CuIn_7Se_{11}$ layers exfoliated. As fabricated FET was used for EDL-FET using ionic liquid, BMIM-PF_6.

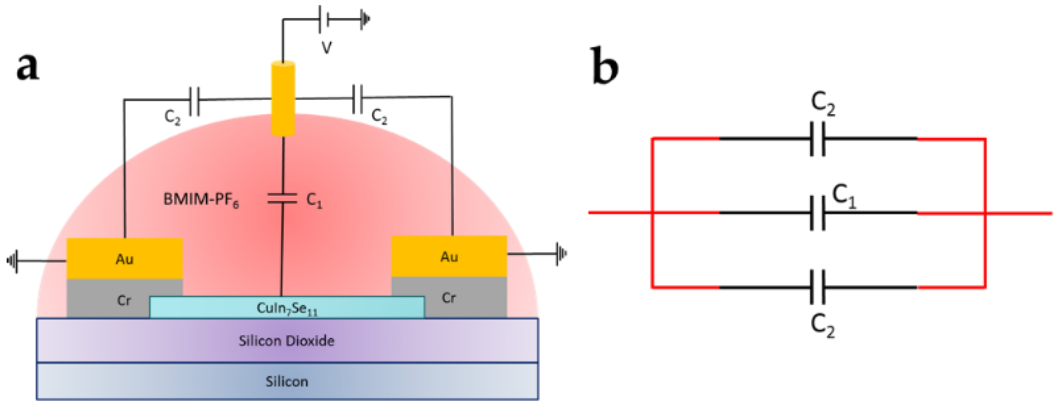

Figure 3.6: a) A schematic of capacitances formed with applied voltage inside ionic liquid. b) An equivalent circuit of schematic shown in a.

3.3.1 Estimation of electric double layer capacitance

As mentioned before, it is crucial to estimate EDL capacitance in order to evaluate performance of EDL-FET accurately. We have used Mott-Schottky analysis to estimated EDL capacitance. It was assumed that ionic liquid will form two different types of EDL depending on surface, *i.e.* EDL formed on gold pad will be different from EDL formed on $CuIn_7Se_{11}$. A schematic of capacitances formed with applied voltage inside ionic liquid is shown in figure 3.6. A capacitance, C_1, indicates EDL formed on $CuIn_7Se_{11}$ and capacitance, C_2, indicates EDL formed on gold surface. This capacitance are parallel to each other and total capacitance of system would be $C_{tot} = C_1 + 2C_2$, where factor of 2 comes since there are two pads that take part

in EDL formation. An equivalent circuit is shown in figure 3.6b. For a device that we have measured, we have used area of gate electrode to be much larger that area of device plus contacts, thus eliminating gate effects from limiting capacitance formed. Also, due to experimental limitations, we have used three gold pads while making a contact with device.

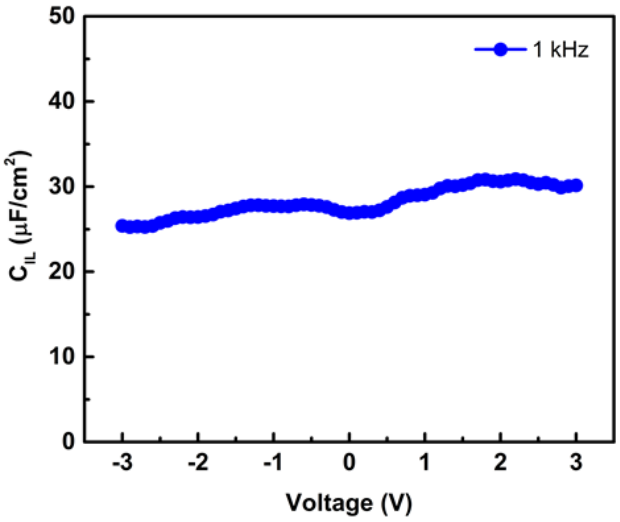

Figure 3.7: Total capacitance, C_{tot}, plotted as a function of applied voltage at 1 kHz frequency.

In order to use Mott-Schottky method, we have connected source and drain terminal of FET, thus making it a short and using as a single electrode. Using Mott-Schottky method, $(1/C_{tot})^2$ was calculated as a function of applied voltage, V, which was converted to total capacitance, C_{tot} as plotted as a function of applied voltage, as shown in figure 3.7. A total capacitance, C_{tot}, was found to be constant at 25 μF cm^{-2}. We have used value of capacitance, C_2, due EDL formed at gold pad to be 7.5 μF cm^{-2}, as shown in literature previously [98]. Thus, capacitance, C_1, was estimated to be 2.5 μF cm^{-2} and it is similar to previously reported values of EDL capacitance formed by BMIM-PF_6 [97] and this value will be used in following section to evaluate figure of merits.

3.3.2 Output and transfer characteristics of EDL-FET

Output and transfer characteristics of $CuIn_7Se_{11}$ EDL-FET is shown in figure 3.8. Output

characteristics, shown in figure 3.8a, indicates 'ohmic-like' contacts, similar to those of back gate characteristics. Transfer characteristics shows typical n-type electrical transport and it is shown in figure 3.8b. It is to be noted that hysteresis is significantly negligible indicating absence of charge trap states at $CuIn_7Se_{11}$ and BMIM-PF_6 interface. A maximum drain current of 7.4 µA was observed in on-state of FET and drain current of 1-5 nA was observed in off-state of FET. It is to be noted that gate leakage current was limited to 10 nA (at highest applied gate voltage of + 2.5 V) and it is 3 order of magnitude less than on-state current. Gate leakage current due to BMIM-PF_6 gate is an order of magnitude higher than that of SiO_2 gate, which might be due to mobile ions in BMIM-PF_6. Leakage current can be further reduces by either using polymer gel as matrix for ionic liquid or by freezing movement of ions by external forces like reducing temperature.

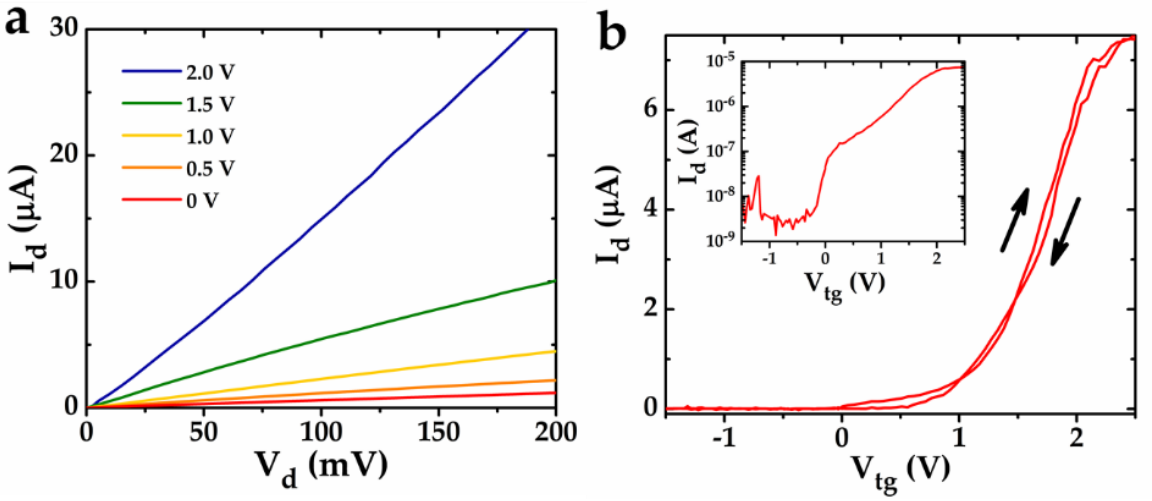

Figure 3.8: a) Output characteristics under different top gate bias conditions (0 V ≤ V_{tg} ≤ + 80 V) are shown. b) A transfer characteristics of $CuIn_7Se_{11}$ FET for forward cycle and reverse cycle using top gate. Inset: Transfer characteristics for forward cycle in log scale for drain current.

3.3.3 Figure of merits: mobility, subthreshold swing, on/off ratio

We have used forward cycle of transfer curve to estimated figure of merits. A threshold voltage was found to ~ 1.2 V. Field effect mobility was calculated from linear region of transfer

curve (superthreshold region) using Eq. 2.3. Device under investigation has the channel length, L, of ~ 10 μm and the channel width, W, of ~ 17 μm. The EDL capacitance, $C_{EDL} \approx 2.5$ μF cm^{-2} was estimated using Mott-Schottky analysis described earlier. A constant drain voltage (V_d) of 0.1 V is applied throughout measurement. A transconductance, g_m, of ~ $4.3 * 10^{-6}$ S was estimated. The room temperature field effect electron mobility of $CuIn_7Se_{11}$ EDL-FET was estimated to be μ_{FE} ~ 17.73 cm^2 V^{-1} s^{-1} which order of magnitude higher than field effect mobility estimated using back gate ($\mu_{FE} \approx 2.66$ cm^2 V^{-1} s^{-1}).

Our measurements shows on-state current, I_{on} ~ $7.4 * 10^{-6}$ A and off-state current, I_{off} ~ $3 * 10^{-9}$ A. Thus on-off ratio was found to ~10^3, which lies in range of ideal on-off ratio. To calculate subthreshold swing, transfer curve is plotted in logarithmic scale (log with base 10) in inset of figure 3.8b and slope, $\partial \log(I_d)/\partial V_g$ of curve was calculated in subthreshold region. Subthreshold slope was found to 5.2 dec/V which correspond to subthreshold swing, SS of 0.19 V/dev, which is close to ideal SS (60 mV/dec).

3.4 Conclusion

In conclusion, EDL-FET were fabricated using few layers of layered $CuIn_7Se_{11}$ flakes which were mechanically exfoliated from single crystals grown using chemical vapor transport technique. We have successfully incorporated ionic liquid, BMIM-PF_6 as a top gate and FET performance was found to be improved compared to that of SiO_2 as back gate. In particular, field-effect mobility, μ_{FE} was increased from 2.66 cm^2 V^{-1} s^{-1} to 17.73 cm^2 V^{-1} s^{-1}, on-off ratio was increased from ~10^2 to ~10^3, and subthreshold swing, SS was improved from 29.8 V/dev to of 0.19 V/dev. Our characterization shows 'ohmic-like' contacts in both back gate and top gate configuration. Hysteresis in transfer characteristics was found to be significantly negligible, thus indicating absence of charge trap states at $CuIn_7Se_{11}$ and BMIM-PF_6 interface.

CHAPTER 4

PHOTOTRANSISTOR

Photon detection is one of the crucial aspect of current electronics and opto-electronics industry [31]. Photodetector is an optoelectronic device which convert information from optical signals to electrical signals so that it can be processed by standard electronics. Photodetector technology has evolved immensely so that various application are more user-oriented than ever and this application spans huge spectrum such as day to day usage like imagining, spectroscopy to large-scales applications like remote sensing, fiber-optic communications [31]. However, with ever advancing technology, improvement in performance of photodetector is desired. Therefore, present research in advancing photodetector technology focus mainly in two directions, first being investigation of new device architectures and other being exploring new materials systems [31].

Conventionally silicon is used as active material for photodetector and silicon photodetectors can be easily integrated into complementary metal oxide semiconductor (CMOS) technology, thus minimizing cost, profiting from scalability and expanding to wide range of applications. However bulk silicon suffers major limitation as light absorbing material as it has indirect band gap of 1.1 eV, limiting light absorption in visible and near-infrared region of electromagnetic spectrum and minimizing light absorbing efficiency [31]. In order to achieve significant response from silicon photodetector, thick channels of silicon have been integrated in commercially available photodetectors. Also, bulk silicon is brittle making the use of silicon in bendable devices unfeasible. Other 3D materials such as InGaAs and their heterostructures have been explored as active material in photodetectors but they shares similar drawbacks as of silicon, with added and further adding fabrication complexity, cost and scalability issues.

Recently, novel nanostructured materials attracted attention due to their extraordinary electrical, optical and mechanical properties. Some of these properties are perhaps needed to overcome limitation of bulk silicon photodetectors. In particular, Si nanowires are used as photodetectors [99] and silicene (single layer of silicon atoms) has been successfully used to fabricate FET [100]. Thus opening doors for Si-based nanostructures for opto-electronics applications. Apart from Si-based nanostructures, various other material systems have been explored as active materials for photo-detection. For example, quantum dots were shown to have substantial photo-detection in the visible, the near infrared, and the short-wavelength infrared region of electromagnetic spectrum [101,102], perovskites based opto-electronics devices tend to have higher efficiencies and narrow band photo detection [103,104], various organic molecules and polymer are also being investigated due to their low fabrication cost and tunable performance [105,106], and carbon nanotubes for nano-scale light sources, photodetectors and photovoltaic devices [107,108].

In this regard, 2D materials have an advantage over other nano-structured materials from practical and fundamental point of view. Atomically thick (few layers) of 2D materials are almost transparent, making them a potential candidate for wearable electronics and photovoltaic devices integrated in a wide variety of niche applications. In 2D materials Quantum confinement in out-of-plane direction results in strong bound excitons, increased absorption efficiency and band gap modulation resulting in tunable optical absorption edge [30,109-111]. Graphene and other semiconducting 2D materials such as transition metal dichalcogenides (TMDs), group III-VI layered materials, black phosphorus and their heterostructures were investigated as active materials for photo-detection [31,112-115].

Here, I will report on the investigations carried out towards two-dimensional layers of

copper indium selenide ($CuIn_7Se_{11}$) FET as an active material for photodetector. We have integrated photodetector in FET structure, as a phototransistor, so that it gives additional degree of freedom to control photo detection mechanism. A detailed review of photocurrent generation and photo response is also presented.

4.1 Introduction to Photodetector and Phototransistor

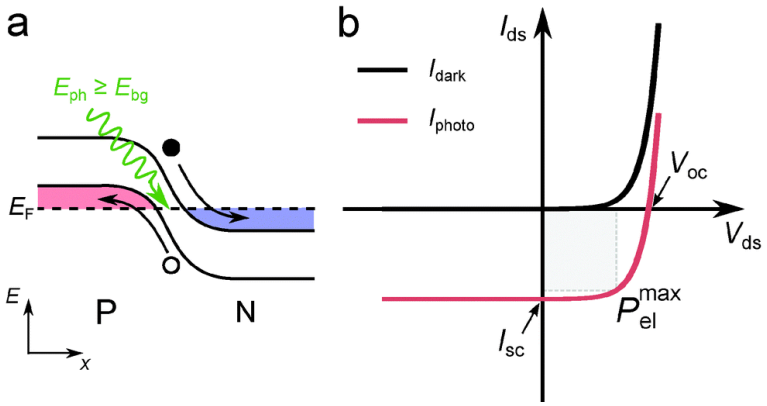

Figure 4.1: A schematic representing photovoltaic effect. a) Band diagram of p-n junction. b) Output characteristics, I_d-V_d, of a typical photodiode. Reproduced from Ref. [115] with permission from the Royal Society of Chemistry.

There are two types of photodetectors that are commonly used, photodiodes and photoconductors. In photodiode, photo generated electron-hole pair are separated by internal electric field and this photocurrent generation mechanism is known as photovoltaic effect. Internal electric field can be originated due to p-n junction between oppositely doped semiconductors, or a Schottky barrier at junction between doped semiconductor and metal, as shown in figure 4.1a. For photodiode, output characteristics, I_d-V_d, curve was found to be nonlinear, figure 4.1b. Under dark condition, drain current, I_d, depends exponentially on drain source voltage, V_d, in forward bias mode (typically $V_d > 0$) and drain current, I_d, negligibly small in reverse bias mode (typically $V_d < 0$), until junction breakdown. Under light illumination and zero external bias ($V_d = 0$), photo generated e-h pair drives a significant photocurrent, known as

short circuit current, I_{sc}. For open circuit, accumulation of charges at opposite ends generates a voltage, known as open circuit voltage, V_{oc}. Since photocurrent flows opposite of drain-source current, I_d-V_d curves under illumination appears to be shifted downward with respect to dark curve. Under illumination, part of I_d-V_d curve appears in fourth quadrant *i.e.* negative current and positive voltage, which is used to generate electrical power, P_{el}^{max}. Usually photodiodes are operated under zero bias for lower dark current and higher detectivity (photovoltaic mode) or under reverse bias for increasing speed of photodiode by lowering junction capacitance (photoconductive mode). Under large reverse bias, strong junction electric field gives enough energy for photo generated carrier to initiate multiplication thus giving multiple carrier per single photon and provides large internal gain. This is known as avalanche photodiode, APD.

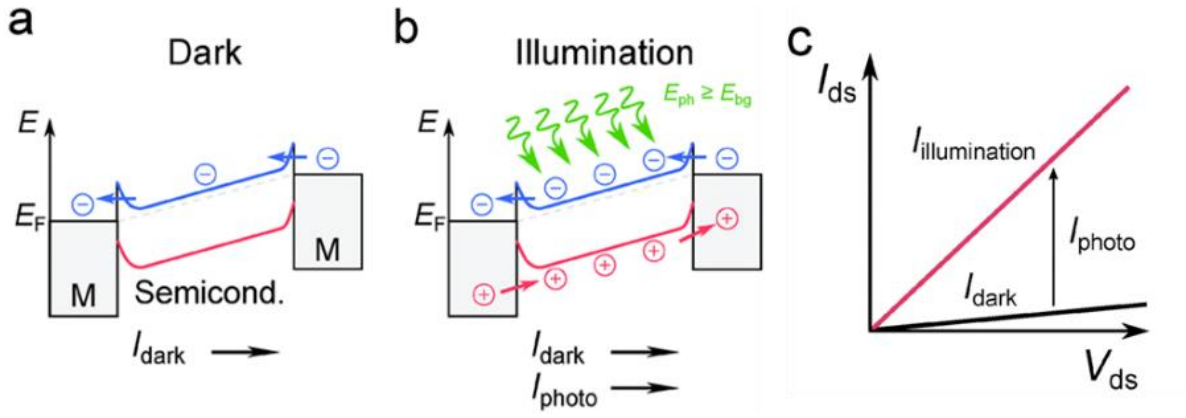

Figure 4.2: A schematic representing photoconductive effect. Band diagram of semiconductor a) before light illumination and b) after light illumination. c) Output characteristics, I_d-V_d, of a typical photoconductor. Reproduced from Ref. [115] with permission from the Royal Society of Chemistry.

In photoconductor, absorbed photon generated extra free carriers which are separated by applied drain-source voltage, V_d. Photo generated carriers increases charge carrier density which increased conductivity of channel (or reducing electrical resistance), and this photocurrent generation mechanism is known as photoconductive effect, shown in figure 4.2. Photoconductive effect is demonstrated by band diagram of photoconductor without and with light illumination in

figure 4.2a and 4.2b, respectively. Under dark condition and applied drain voltage bias, V_d, a small drain-source current, I_d, flows which is also known as dark current, I_{dark}. Under illumination, absorption of photon with higher energy than bandgap ($E_{ph} > E_{bg}$) generated electron-hole pair which drift in opposite direction, resulting in net increase in current, knows as photocurrent (I_{ph}) and it is shown in output characteristics curve of photoconductor in figure 4.2c. If hole mobility is much significantly lower than electron mobility, photo generated electron can flow through channel much faster than phot generated hole thus leading to photoconductive gain and quantum efficiency larger than one *i.e.* more than one electron can be extracted from single photon

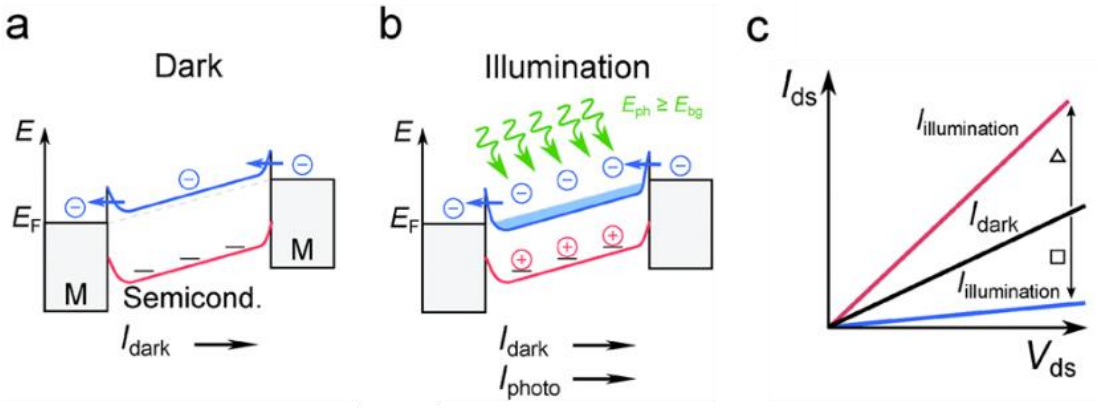

Figure 4.3: A schematic representing photogating effect. Band diagram of semiconductor a) before light illumination and b) after light illumination. c) Output characteristics, I_d-V_d, of a typical photoconductor. Reproduced from Ref. [115] with permission from the Royal Society of Chemistry.

A photogating effect is a subset of photoconductive effect, where photo generated electrons or holes are trapped in localized state, thus acting as local gate and modulating resistance of channel, as shown in figure 4.3. Photogating effect is demonstrated by band diagram of photoconductor without and with light illumination in figure 4.3a and 4.3b, respectively. A large lifetime of localized trap states leads to large photoconductive gain. Usually trap states with long lifetime are located at defects or at surface of semiconductor, thus

photogating effect is important in nanostructured materials based photoconductors, where surface states plays important role in electrical properties. Contrary to photoconductive effect which result in positive photocurrent, photogating can result in positive and negative photocurrent based on trapped carrier type [115]. A typical output characteristics is shown in figure 4.3c. Assume that trap states are present near valence band, as shown in figure 4.3a, thus only holes can be trapped. If majority carriers are electron then photocurrent will be positive since holes are trapped and not available for recombination, resulting in longer lifetime for electron. Also electric field of trap states will shift fermi level close to conduction band, inducing more electrons. If a majority carriers are holes then photocurrent will be negative since trapped holes will shift fermi level away from valence band, resulting in decrease in current.

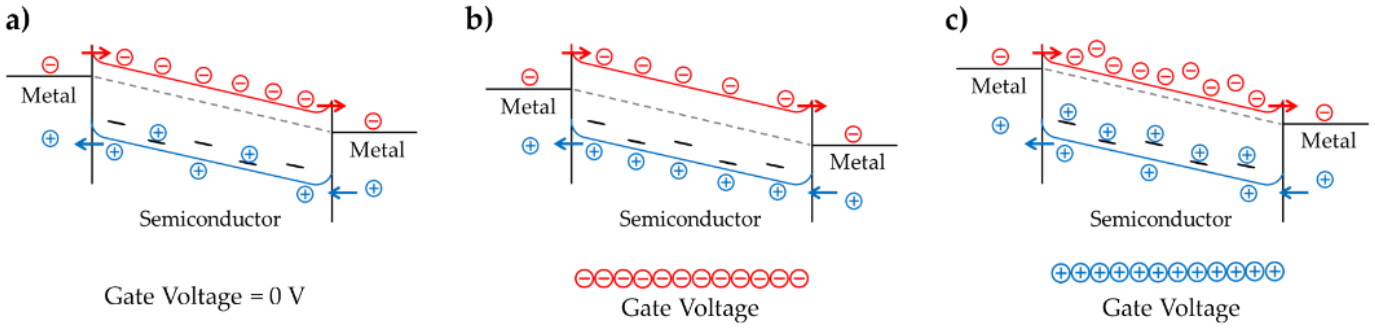

Figure 4.4: Band diagram of typical phototransistor a) without application of gate voltage, b) with negative of gate voltage and c) with positive of gate voltage.

In practical photodetector, photoconductive effect and photogating effect can be indistinguishable and occurs simultaneously in device, as shown in figure 4.4a. However dissimilarity in their time scale can be used to distinguish signal coming from photoconductive and photogating effect [116]. Having a third contact for photoconductor, as a gate electrode in FETs, can be useful in controlling photoconductive and photogating effect and to some extend disengage them [45]. A gate controlled photocurrent generation mechanics can be demonstrated

by band diagrams of photoconductor, shown in figure 4.4b and figure 4.4c. Assuming that trap states are present near valence band as shown in figure 4.3a, when a negative gate voltage is applied, trapped holes are pulled back to valence band thus making trapping ineffective and photoconductive effect will be dominated. When positive gate voltage is applied, holes are pushed into traps states, thus shifting fermi level close to conduction band which result in more electrons in conduction band and photogating effect will be dominated. Thus by simply applying gate voltage, photocurrent generation mechanism can be controlled, making phototransistors (photoconductor integrated into FET) a promising device architect to investigate fundamental properties.

Other than above mentioned photocurrent generation mechanisms, photocurrent can also be generated through thermal mechanisms. A temperature gradient induced by non-uniform heating under light illumination can result in photocurrent, known as photo-thermoelectric effect. On the contrary, a homogenous temperature change due to light illumination modify resistivity of material, known as photo-bolometric effect. However any contributions that might arise from this thermal effects can be neglected by employing laser with a larger spot size than device. Here, we have used laser with spot size of diameter ~ 2.8 mm which is 2 orders higher that typical device dimensions (~ few tens of μm).

As photodetectors can be employed with different working principles, different materials, and different geometries, a traditional set of figures of merits are used. Here I have used responsivity (R), external quantum efficiency (EQE), response time (τ_{90-10}), bandwidth (f_{3dB}), noise equivalent power (NEP) and specific detectivity (D*) as a figure of merits for $CuIn_7Se_{11}$ phototransistors. A typical figure of merits values for commercially available Si and/or InGaAs photodiodes are also presented.

Responsivity, R, is a ratio of photocurrent generated, I_{ph}, to total incident power on photodetector. When laser spot size is significantly larger that device, effective power, P_{eff}, ($P_{eff} = P_{in} * A_{dev} / A_{spot}$) is used instead total incident power, P_{in}, where A_{dev} and A_{spot} are device area and area of laser spot, respectively. Responsivity is defined in Eq. 4.1 as follows,

$$R = \frac{I_{ph}}{P_{eff}} \quad \text{.....Eq. 4.1}$$

Note that responsivity depends on external bias voltage and other geometric factors. A commercial Si photodiodes, $R \approx 500$ mA W^{-1} at wavelength, $\lambda = 880$ nm and a commercial InGaAs photodiodes, $R \approx 1.2$ A W^{-1} at wavelength, $\lambda = 1550$ nm.

External quantum efficiency, EQE, is a ratio of number of charge carrier in photocurrent, n_e to the total number of photon incident, n_{ph}. External quantum efficiency, EQE, is related to Responsivity, R, with Eq.4.2 as follows.

$$EQE = R \frac{h\,c}{e\,\lambda} \quad \text{.....Eq. 4.2}$$

where, h is Plank's constant, c is speed of light, e is charge of electron and λ is illuminated light wavelength. EQE is usually presented in percentage. Thus, EQE > 100 % implies that more than one charge carrier was generated per single photon incident. For commercial Si photodiodes, EQE is in order of $\sim 6 * 10^5$ %.

Response time, $\tau_{90\text{-}10}$ (or $\tau_{10\text{-}90}$) for a photodetector can be defined as the time required for the photocurrent value to drop from 90% to 10% (or rise from 10% to 90%) of its saturated photocurrent value during fall cycle (or rise cycle). A commercial Si and InGaAs photodiodes shows response times of ~ 50 ps. Usually, $\tau_{90\text{-}10} > \tau_{10\text{-}90}$ as fall response time depends on various factors such as presence of trap states, recombination dynamics whereas rise response time depends primarily on generation of electron-hole pair. A small response time is desired for

certain application where functionalities such as fast photo switching are needed. A commercial Si photodiodes and a commercial InGaAs photodiodes have a response time of ~ 100 ps.

Bandwidth, B or f_{3dB}, of photodetector is defined as modulation frequency of incident light signal at which detector signal power is half (or amplitude is 70%) of its value under continuous illumination. Bandwidth of a commercial Si and InGaAs reaches few tens of GHz. Here we have used photocurrent, I_{ph}, as a detector signal amplitude.

Noise equivalent power, NEP, is defined as input signal power that gives signal to noise ratio 1 at 1 Hz output bandwidth. In other words, NEP essentially represents minimum detectable power. Total noise present in system will determine the NEP and the total noise consist of shot noise from dark current, Johnson noise, and thermal fluctuation noise. Usually shot noise dominates in the total noise, thus NEP can be given as Eq 4.3.

$$\mathrm{NEP} = \frac{\sqrt{2\ \mathrm{e}\ \mathrm{I_{dark}}}}{\mathrm{R}} \qquad \text{Eq. 4.3}$$

Thus detectors with small dark current and large responsivity will have small NEP. A commercial Si photodiodes have a NEP of ~ 10^{-14} W $Hz^{-1/2}$ and a commercial InGaAs photodiodes have a NEP of ~ 10^{-15} W $Hz^{-1/2}$.

Specific detectivity, D*, is derived from noise equivalent power, NEP, area of photodetector, A, and bandwidth of photodetector, B, as shown in Eq 4.4.

$$\mathrm{D^*} = \frac{\sqrt{\mathrm{A\ B}}}{\mathrm{NEP}} \qquad \text{Eq. 4.4}$$

Advantage of using specific detectivity over NEP is that the specific detectivity values are normalized with detector's active area and bandwidth, thus comparison between detectors with different active areas and bandwidth can be accomplished. A detectivity of Si photodiode is in order of ~ 10^{12} Jones or cm $Hz^{1/2}$ W^{-1}.

4.2 Experimental Section

FET were fabricated and characterized as described in chapter 2. In order to explore opto-electronics properties, FET were exposed to continuous laser illumination of wavelength, λ = 658 nm which correspond to energy, E = 1.88 eV and tunable laser illumination intensity. A laser with spot size of diameter ~ 2.8 mm were used in experiments. A maximum incident laser intensity achieved by laser is P_{in} = 60 mW. Laser intensity, P_{in}, that used in experiments were 2 mW, 5 mW, 10 mW, 20 mW, 30 mW, 40 mW, 50 mW and 60 mW. Since spot size of laser ~ 2.8 mm is 2 orders higher that typical device dimensions (~ few tens of μm), effective power, P_{eff}, were used to evaluate performance for accurately estimations. Effective power on device, P_{eff}, were estimated by assuming constant distribution of laser intensity within laser spot, using formula $P_{eff} = P_{in} * A_{dev} / A_{spot}$, where P_{in}, A_{dev} and A_{spot} are total incident power, device area and area of laser spot, respectively. For a device that was used as a phototransistor, a device area was estimated to be $A_{dev} = 1.5 * 10^{-10}$ m^2. Corresponding effective power, P_{eff}, for a device were 0.049 μW, 0.123 μW, 0.246 μW, 0.492 μW, 0.738 μW, 0.984 μW, 1.23 μW, and 1.48 μW. All experiments were carried out at drain-source voltage of V_d = 0.2 V.

To determine photoresponse dynamics of $CuIn_7Se_{11}$ phototransistor, the laser was modulated using a function generator (BK Precision 4011A), with frequencies varying from 1 Hz to 200 kHz. The time dependent photo-current was converted into the time dependent voltage using current-voltage converter (Keithley 428 current amplifier) and the resultant time dependent voltages was recorded by a digital oscilloscope (Rigol, DS2072A).

4.3 Results and Discussions

As fabricated FET were characterized using techniques described in chapter 2. Transfer and output characteristics is shown in figure 4.5. Device performance were found to be similar.

Briefly, electronic transport shows n-type behavior. Output characteristics shows 'ohmic-like contact' within applied voltage regime. Transfer characteristics shows field-effect mobility, μ_{FE} of 24.6 $cm^2\ V^{-1}\ s^{-1}$, on-off ratio of ~ 10^4, and subthreshold swing, SS of 1.6 V/dev. This as fabricated FET was used as phototransistor.

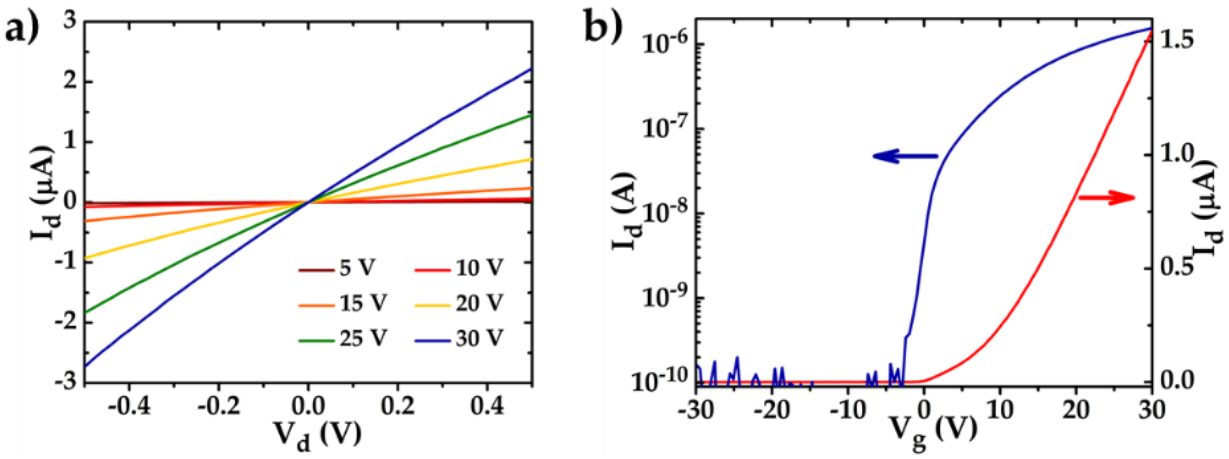

Figure 4.5: a) Output characteristics under different gate bias conditions are shown. b) A transfer characteristics of $CuIn_7Se_{11}$ FET for forward cycle. This as fabricated FET was used as phototransistor.

4.3.1 Photo-response of phototransistor

Photo-response of a phototransistor is shown in figure 4.6. Output characteristics *i.e.* drain current, I_d, response with applied drain voltage, V_d, is shown in figure 4.6a. Increase in drain current, I_d, can be attributed to photo-generated electron-hole pairs being more effectively separated and captured with enhanced carrier drift velocity, resulting in decrease in carrier transit time, $t_r = L^2 / \mu V_d$, where L is channel length and μ is carrier mobility [117]. Also, linearity of I_d-V_d curve reasoned to absence of p-n junction in semiconductor or Schottky barrier at contact. Thus photovoltaic effect is nonexistent in $CuIn_7Se_{11}$ phototransistor. I_d-V_d curves are found to be intersecting at (0, 0), implying that thermal mechanisms plays no role in generating photocurrent. Besides, with the maximum effective laser power on the device, P_{eff}, utilized in our measurement

is ~ 10^{-2} μW/μm^2, which is significantly small for generating an appreciable voltage drop across channel. Thus $CuIn_7Se_{11}$ phototransistor behaves as a pure photoconductor and generated photocurrent might be due to photoconductive and/or photogating effect.

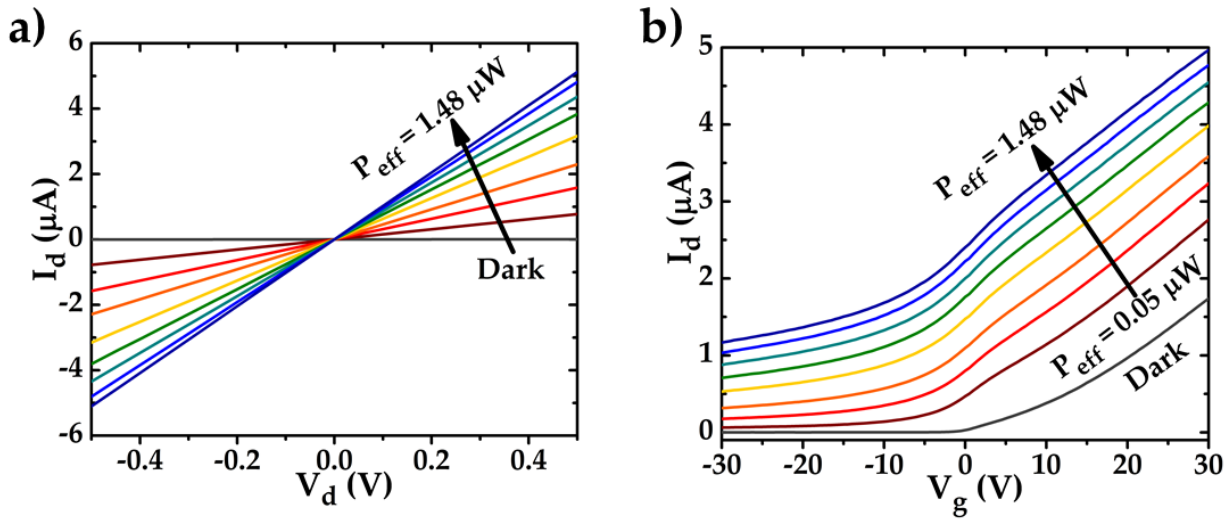

Figure 4.6: a) Output characteristics under different effective laser power and at zero gate voltage are shown. b) A transfer characteristics under different effective laser power and with constant drain bias, V_d, of 0.2 V is shown

Figure 4.6b shows transfer characteristics of $CuIn_7Se_{11}$ phototransistor i.e. dependence of drain current, I_d, on gate voltage, V_g, under different effective laser powers, P_{eff}. Under dark conditions, off-state current was found to ~ 100 pA and on-state current was found to be ~ 1.7 μA at gate voltage, V_g = + 30 V. Under maximum effective laser power, P_{eff} = 1.48 μW, off-state current was found to be increased to ~ 1.7 μA at gate voltage, V_g = - 30 V and on-state current was increased to ~ 5 μA at gate voltage, V_g = + 30 V. Increment in off-state and on-state current is a common feature of photoconductor and similar behavior can be observed in 2D materials based photodetectors. The gate leakage current was approximately constant throughout all laser intensities used in the experiments indicating increment in drain current is due to photo carrier generation and the gate leakage current does not play any role.

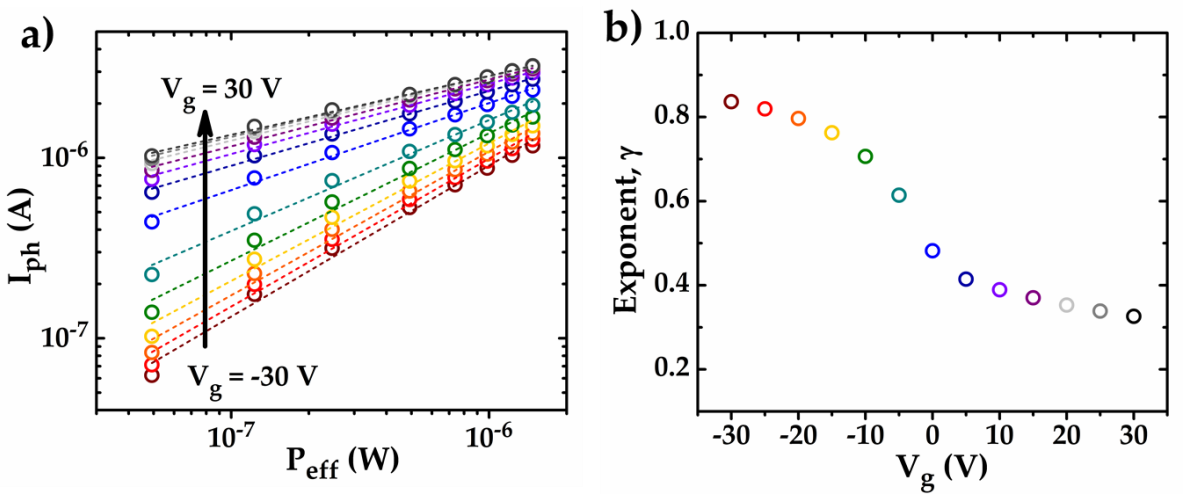

Figure 4.7: a) Variation of I_{ph} as a function of effective laser poser (plotted in log-log scale) and at different gate voltages (V_g from -30 V to +30 V with 5 V increment) is shown. b) Variation of power exponent (γ) as function of gate voltage, color coded w.r.t. a.

To shed more insight on photocurrent generation mechanism, photocurrent, I_{ph}, was plotted with effective laser power, P_{eff}, at different gate voltage, V_g, in figure 4.7a. Photocurrent was found to be following power law fit, $I_{ph} \propto (P_{eff})^{\gamma}$, where γ is power exponent. In case of pure photo-conductive effect, photocurrent, I_{ph}, is linearly dependent on the incident photon flux by the equation $I_{ph} = \Gamma\, \eta\, e\, G$, [118] where Γ is number of absorbed photons per unit time, η is internal quantum efficiency, e is electron charge and G is photoconductive gain. Several theoretical models have been proposed to explain significant deviation from linearity [119]. For nanostructured devices, these deviation can be explained on the basis of charge trap states. Photo generated charge carrier are trapped in relatively long lived trap states and act as local gate, this phenomena is known as photogating effect. For zero gate voltage, $V_g = 0$ V, power exponent, γ, is ~ 0.5, which correspond to bimolecular recombination process [120]. Variation of power exponent, γ, with gate voltage, V_g, is shown in figure 4.7b. It was found that exponent decreases from 0.83 in the off-state to 0.33 in the on-state. Such a dependence of exponent was explained by changeover in fundamental photocurrent generation mechanism from nearly pure

photoconductive effect at negative gate voltage ($\gamma \rightarrow 1$) to photogating dominated photoconductive effect at positive gate voltage ($\gamma < 1$) [45].

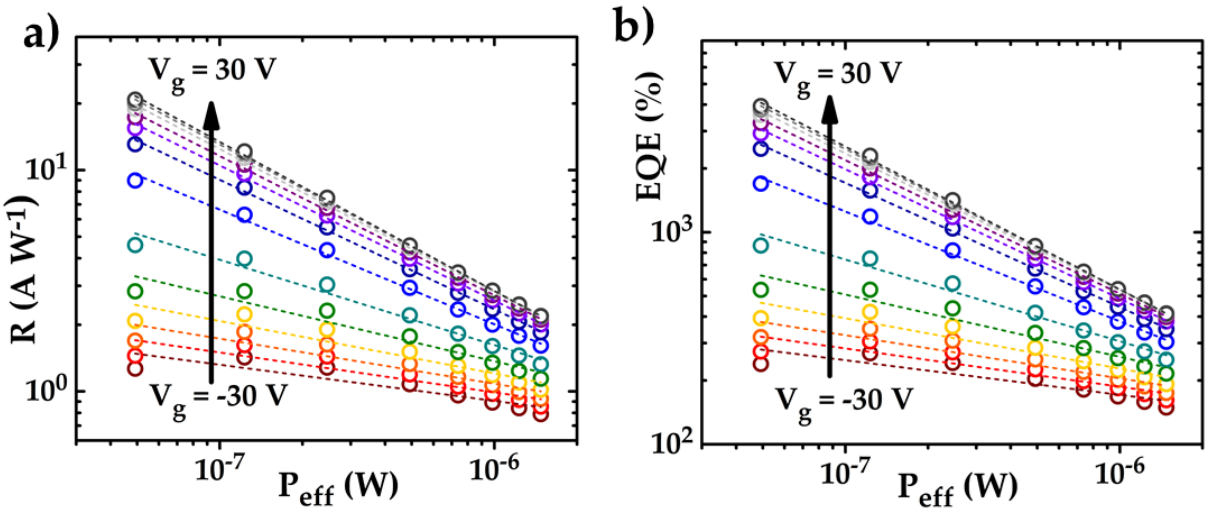

Figure 4.8: a) Variation of R and b) EQE % as a function of effective laser power (plotted in log-log scale) and at different gate voltages (V_g from - 30 V to + 30 V with 5 V increment) is shown.

4.3.2 Figure of merits: responsivity, external quantum efficiency

Variation of responsivity, R, with effective laser power, P_{eff}, at different gate voltage, V_g, in figure 4.8a. A responsivity was found to be R ≈ 9 A W^{-1} at zero gate voltage, V_g = 0 V and effective laser power, P_{eff} = 0.049 μW, which is significantly higher than that of commercially available Si and InGaAs photodiodes and higher or comparable with previously reported group III-VI layered materials [34,44,121-124]. Responsivity can be further improved to R ≈ 21 A W^{-1} upon application of gate voltage, V_g = + 30 V at effective laser power, P_{eff} = 0.049 μW. Additionally, responsivity can be tuned and increased by at least an order of magnitude by application of a gate voltage and/or increased source-drain bias. For example, responsivity, R can be increased from R ≈ 9 A W^{-1} to R ≈ 60.6 A W^{-1} by increasing drain voltage, V_d, from V_d = 0.2 V to V_d = 2 V at zero gate voltage, V_g = 0 V and effective laser power, P_{eff} = 0.049 μW.

Figure 4.8b shows variation of external quantum efficiency, EQE, with effective laser power, P_{eff}, at different gate voltage, V_g. A maximum EQE of $\approx 4 * 10^3$ % was achieved correspond to effective laser power, P_{eff} = 0.049 μW and gate voltage, V_g = + 30 V. EQE exceeding 100 % suggest that multiple photo carriers are generated per single incident photons and it is reasoned to excitation energy higher than the band-gap or presence of internal gain mechanism such as photo-gating [45,115].

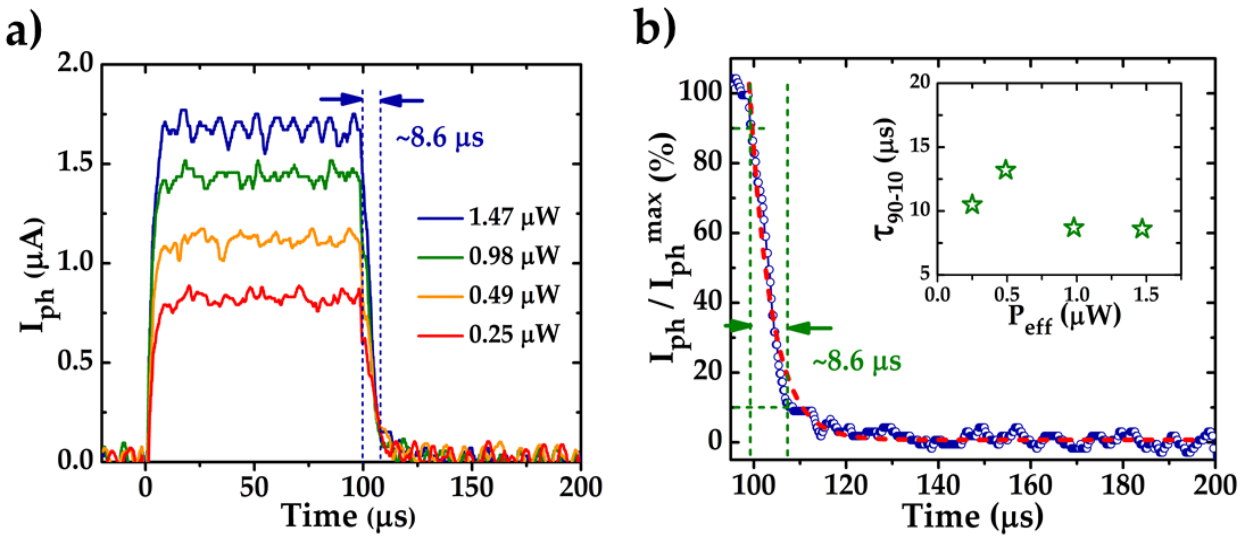

Figure 4.9: a) Time dependent photocurrent for varying effective laser power is shown. b) A falling edge of time dependent photocurrent is shown at effective laser power of P_{eff} = 1.48 μW. (Inset) response times as a function of effective laser power is shown.

4.3.3 Photo-response dynamics: response time, specific detectivity

Photo-response dynamics of $CuIn_7Se_{11}$ phototransistor was investigated in order to achieve industrial implementation. Time dependent photocurrent was shown in figure 4.9a at different effective laser power, P_{eff}. A response time, τ_{90-10}, was found to be ~ 8.6 μs at effective laser power, P_{eff} = 1.48 μW. A response time was found to almost constant, ~ tens of μs for a different effective laser powers, shown inset of figure 4.9b. Response time of $CuIn_7Se_{11}$ phototransistor is comparable with response time of SnS_2 photodetector where $\tau_{on/off}$ ~ 5 μs, [49]

which is fastest response among 2D materials currently reported and several orders of magnitude faster than previously reported group III-VI layered materials [33,34,38,44-46,122,125]. A falling edge of time dependent photocurrent is shown in figure 4.9b, here photocurrent is normalized with maximum photocurrent (I_{ph}^{max}) as I_{ph}/I_{ph}^{max}. Further, photocurrent was fitted with exponential decay, with Eq. 4.5

$$\frac{I_{ph}}{I_{ph}^{max}} = A * e^{-t/\tau_c} \quad \text{.....Eq. 4.5}$$

where, A is fitting constant, τ_c is time constant which gives intrinsic time scale. Here we found that time constant, τ_c is = 4.8 μs.

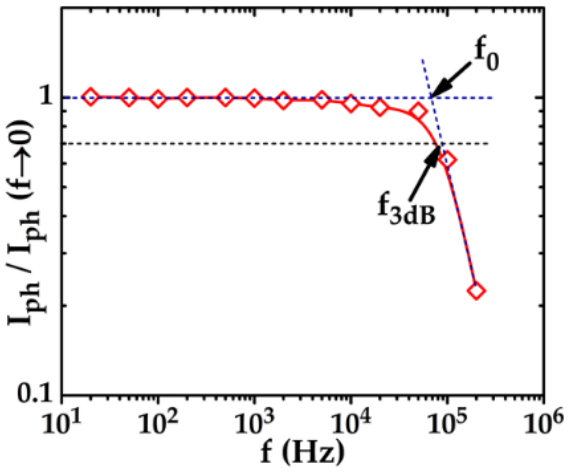

Figure 4.10: Normalized photocurrent with varying laser modulation frequency.

To determine bandwidth of a photodetector, we modulated laser using function generator, with varying frequencies from 1Hz to 200 kHz. Photocurrent was further normalized with photocurrent with continuous illumination, I_{ph} (f→0) and plotted as a function of modulation frequency in figure 4.10. Photocurrent starts to decrease drastically after a certain frequency, known as characteristic roll over frequency, f_0. Here we found characteristic roll over frequency, $f_0 \approx 70.6$ kHz, which correspond to characteristic transient time $\tau_0 = 1 / (2 \pi f_0) \approx 2.25$ μs. Further, we estimated 3dB bandwidth, f_{3dB}, as $f_{3dB} \approx 73.4$ kHz and correspond to characteristics

response time $\tau_{3dB} = 1 / (2 \pi f_{3dB}) \approx 2.17$ μs. Note that response time and characteristics response time are similar, suggesting that reactance (due to inductance or capacitance) that are formed at semiconductor-metal junction due to Schottky barrier or other parts in circuit are negligible.

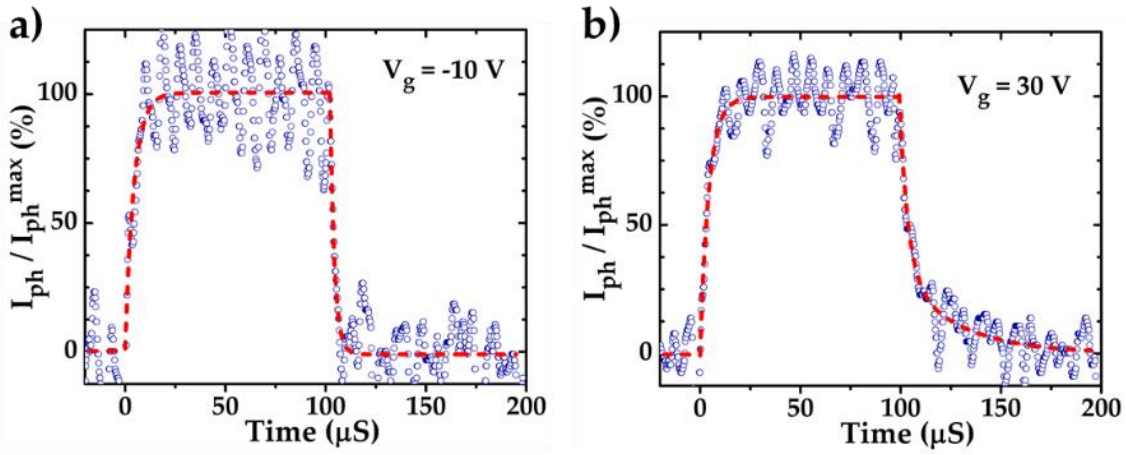

Figure 4.11: Time dependent photocurrent for effective laser power of $P_{eff} = 1.48$ μW, at gate voltages, V_g, of a) - 10 V and b) + 30 V is shown. Red dotted curve denoted fitted curve.

To verify effect of photogating on photocurrent generation, we measured time dependent photocurrent at gate voltage, V_g = - 10 V and V_g = + 30 V, as shown in figure 4.11a and figure 4.11b, respectively. Falling edge of time dependent photocurrent at gate voltage, V_g = - 10 V can be fitted with an exponential decay, Eq. 4.5, with time constant being $\tau_c = 2.2$ μs. Whereas, Falling edge of time dependent photocurrent at gate voltage, V_g = + 30 V can be fitted with a bi-exponential decay, *i.e.* two exponential decays of Eq. 4.5, with time constants being $\tau_{c1} = 4.2$ μs and $\tau_{c2} = 28.9$ μs. It was demonstrated before that, in case of In_2Se_3 [45], initial fast decay correspond to time scale associated with band to band transition whereas later slow decay correspond to time scale associated with charges being trapped and detrapped. Thus, in case of time dependent photocurrent at gate voltage, V_g = - 10 V, there is only band to band transition available and carrier charges are not trapped at trap states, indicating nearly pure photoconductive effect. In case of time dependent photocurrent at gate voltage, V_g = + 30 V, presence of bi-exponential decay indicates that photocurrent generation mechanism is

photogating dominated photoconductive effect.

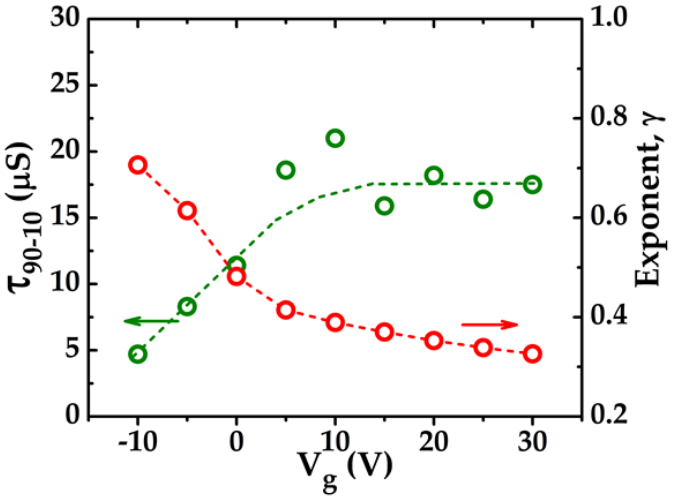

Figure 4.12: Response time (green) and power exponent (red) as a function of gate voltages, V_g.

A response time, τ_{90-10}, is plotted as function of gate voltage, V_g, in figure 4.12. For a comparison purpose, I have plotted power exponent, γ, in same figure. It can be concluded that, for gate voltage, V_g, greater than 5 V, photogating effect is present along with photoconductive effect. Also, rising edge of time dependent photocurrent at gate voltage, V_g = - 10 V and V_g = + 30 V was fitted with exponential rise curve and as hypothesized, time constant, τ_c, was found to be same for both cases, τ_c = 4.4 μs. Similarity in time constant of rising edge indicates that, charge trap states affects recombination of electron-hole and does not influence generation of electron-hole.

To sum up photoresponse of $CuIn_7Se_{11}$ phototransistor, we measured noise equivalent power, NEP, and specific detectivity, D*, and it is shown in figure 4.13a and figure 4.13b, respectively. We found that minimum noise equivalent power, NEP, of 1.1 * 10^{-14} W $Hz^{-1/2}$, which correspond to specific detectivity, D*, of 3.04 * 10^{11} Jones, at effective laser power of, P_{eff} = 0.049 μW and gate voltage, V_g = 0 V. This values of NEP and specific detectivity are comparable with that of commercial photodiodes. We also found that, modifying parameters such as drain voltage could enhance NEP and detectivity. For example, noise equivalent power,

NEP, can be increased from NEP ≈ 1.1 * 10^{-14} W $Hz^{-1/2}$ to NEP ≈ 1.06 * 10^{-15} W $Hz^{-1/2}$ and specific detectivity, D*, can be increased from D* ≈ 3.04 * 10^{11} Jones to D* ≈ 3.15 * 10^{12} Jones by increasing drain voltage, V_d, from V_d = 0.2 V to V_d = 2 V at zero gate voltage, V_g = 0 V and effective laser power, P_{eff} = 0.049 μW.

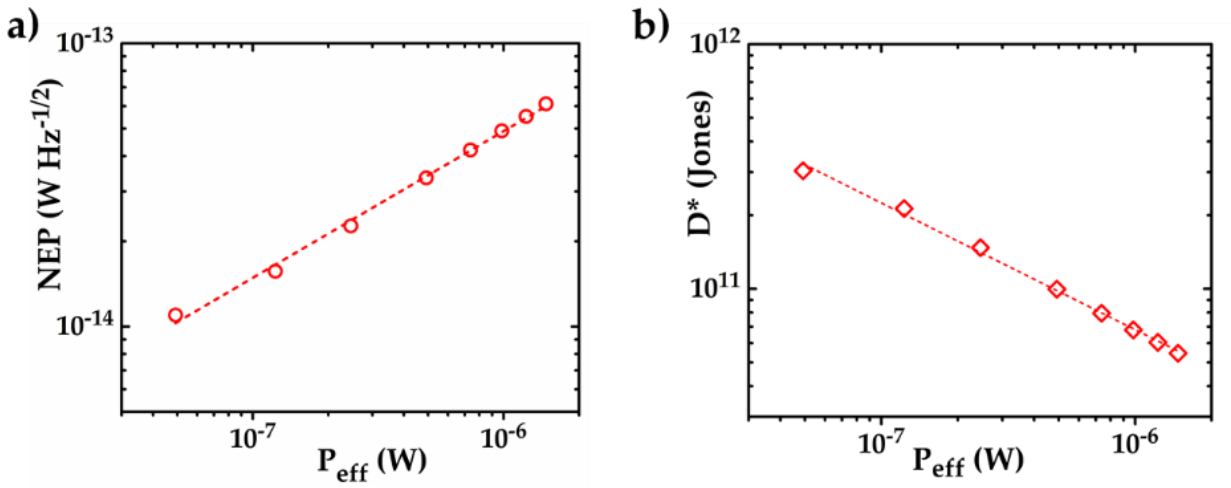

Figure 4.13: a) Variation of noise equivalent power, NEP and b) specific detectivity, D* as a function of effective laser power (plotted in log-log scale) at zero gate voltage is shown.

4.4 Conclusion

In conclusion, photogating dominated photoconductive effect was observed in $CuIn_7Se_{11}$ phototransistor. Some fundamental aspects regarding photocurrent generation mechanism were studied and controlled by back gate voltage. Nearly pure photoconductive effect at negative gate voltage ($\gamma \rightarrow 1$) and photogating dominated photoconductive effect at positive gate voltage ($\gamma < 1$) was observed and further confirmed by time-dependent photocurrent. Several parameters corresponding to photodetectors such as responsivity, R ≈ 60.6 A W^{-1}, EQE of the order 10^4 %, response time, τ_{90-10} ~ 8.6 μs, characteristics response time τ_{3dB} ≈ 2.17 μs, bandwidth, f_{3dB} ≈ 73.4 kHz, noise equivalent power, NEP ≈ 1.06 * 10^{-15} W $Hz^{-1/2}$ and specific detectivity, D* ≈ 3.15 * 10^{12} Jones were estimated. This parameters can be further tuned by application of gate voltage and drain voltage.

CHAPTER 5

CONCLUSION, SUMMARY AND FUTURE OUTLOOK

Thus in conclusion, we have fabricated $CuIn_7Se_{11}$ field effect transistor using few layers of layered $CuIn_7Se_{11}$ flakes which were mechanically exfoliated from single crystals grown using chemical vapor transport technique. Investigation has been carried out towards exploring fundamental aspects of electron transport and photocurrent generation in semiconducting $CuIn_7Se_{11}$ layers. To our knowledge, this is first time where 2D forms of ternary Copper Indium Selenide have been investigated as a channel material for transistor and photodetector. Some of the extra-ordinary properties shown by $CuIn_7Se_{11}$ FET are summarized below.

To summarize $CuIn_7Se_{11}$ FET's electronic properties, we found ohmic-like contacts with Cr/Au contact having negligible contact resistance when compared to total resistance of device, threshold voltage, V_{th}, being ~ 8.9 V, and some of the figure of merits of FET are field-effect mobility, $\mu_{FE} \approx 36.89$ cm^2 V^{-1} s^{-1}, on/off ratio ~ 10^4, subthreshold swing, SS ≈ 2.44 V/dev, and low-field mobility, μ_0, is 39.91 cm^2 V^{-1} s^{-1}. We also observe presence of charge trap states at $CuIn_7Se_{11}$ and SiO_2 interface with charge trap density of states (DOS) being $N_{tr} \approx 3.1 * 10^{12}$ cm^{-2} eV^{-1}. This electronic properties can be further improved by incorporating ionic liquid, BMIM-PF_6 as a top gate. We have successfully incorporated ionic liquid, BMIM-PF_6 as a top gate and FET performance was found to be improved compared to that of SiO_2 as back gate. In particular, field-effect mobility, μ_{FE} was increased from 2.66 cm^2 V^{-1} s^{-1} to 17.73 cm^2 V^{-1} s^{-1}, on/off ratio was increased from ~10^2 to ~10^3, and subthreshold swing, SS was improved from 29.8 V/dev to of 0.19 V/dev. Hysteresis in transfer characteristics of top gated FET was found to be significantly negligible, thus indicating absence of charge trap states at $CuIn_7Se_{11}$ and BMIM-PF_6 interface. EDL-FETs indicating performance improvement are summarized in table 5.1.

Device #	Mobility ($cm^2 V^{-1} s^{-1}$)		Subthreshold Swing (V/dec)		On/off Ratio	
	Back Gate	Top Gate	Back Gate	Top Gate	Back Gate	Top Gate
Device I	2.66	17.73	29.8	0.19	$\sim 10^2$	$\sim 10^3$
Device II	4.04	21.84	9.6	0.30	$\sim 10^2$	$\sim 10^4$
Device III	0.23	0.42	107	0.81	$\sim 10^0$	$\sim 10^3$

Table 5.1: Key parameters of $CuIn_7Se_{11}$ devices on SiO_2 thickness = 300 nm (device I and III), on SiO_2 thickness = 1000 nm (device II), V_d = 0.1 V (device I and III) and V_d = 1 V (device II) are listed. Also, device III shows preliminary data obtained on ionic gel polymer electrolyte using BMIM-PF_6 as ionic liquid and PEO as gel matrix.

While doing EDL-FETs, we had a hard time conducting experiments due to reactivity and viscosity of ionic liquid. After placing ionic liquid as top gate, SiO_2 used to break down making back gate leak. SiO_2 breakdown might be due to fact that ionic liquid, BMIM-PF_6, being composed purely of ions, reacts with dangling bonds on the surface of SiO_2. We have tried treating SiO_2 with piranha solution [3:1 mixture of sulfuric acid (H_2SO_4) and 30% hydrogen peroxide (H_2O_2)], which neutralizes some of dangling bonds on the surface of SiO_2, but results were unimproved in sense that SiO_2 used to breakdown within first couple runs. In literature people have used polymer gel as a support matrix which helps in keeping ionic liquid immobile, however ions are free to within matrix thus enabling formation of EDLs at solid-electrolyte surfaces. One of the preliminary device is shown in table 5.1 as Device III. This device was fabricated using relatively bulk flake of $CuIn_7Se_{11}$ and first trial of polymer gel electrolyte was conducted on it. Here we have used PEO as polymer gel matrix and BMIM-PF_6 as ionic liquid in 90:10 ratio (by weight).

We found that back gate was not leaking and dual gating (back gate using SiO_2 and top gate using gel polymer electrolyte) was possible. Interconnection between SiO_2 back gate and

ionic liquid top gate, in particular change in threshold voltage, V_{th}, was used to estimate EDL capacitance at device. Note that this method estimates EDL capacitance accurately since only EDL formed on device will shift threshold voltage. Due to bulk nature of device, SiO_2 back gate was not powerful enough to operate FET. Transfer characteristics using back gate is shown in figure 5.1a. We found that field-effect mobility, μ_{FE} of 0.23 $cm^2\ V^{-1}\ s^{-1}$, on/off ratio of ~ 10^0, subthreshold swing, SS of 107 V/dev by using SiO_2 back gate. This values are several orders of magnitude lower that other device presented here. When polymer gel electrolyte was used as a top gate, we found enormous improvement in FET performance.

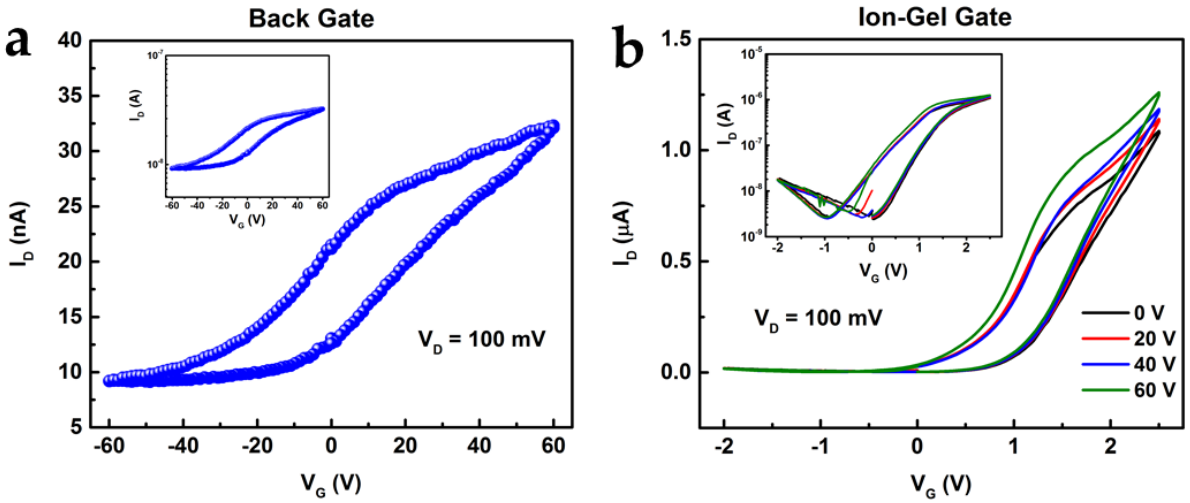

Figure 5.1: a) A transfer characteristics of $CuIn_7Se_{11}$ FET using SiO_2 as back gate. b) A transfer characteristics of $CuIn_7Se_{11}$ FET using top gate in dual gate configuration with constant back gate voltage of V_{bg} = 0 V, 20 V, 40 V, and 60 V

Transfer characteristics using top gate is shown in figure 5.1b. Particularly we found that field-effect mobility, μ_{FE} of 0.42 $cm^2\ V^{-1}\ s^{-1}$, on/off ratio of ~ 10^3, subthreshold swing, SS of 0.81 V/dev by using top gate. Although field effect mobility is increased twice, it is still an order of magnitude lower that other device. However, On/off ratio and subthreshold swing are improved to significantly and comparable with other device. Field field-effect mobility, μ_{FE} was found to be 0.56 $cm^2\ V^{-1}\ s^{-1}$ in dual gate configuration with constant back gate voltage, V_{bg} at 60 V. Shift

in threshold voltage in dual gate configuration was used to compute EDL capacitance and C_{EDL} was found to be 3.4 μF cm^{-2}. Although this are preliminary data, I believe that a very thorough and interesting studies can be done and it will be my first project to start with in Ph.D.

One of the application of EDL-FETs is biosensor or chemical sensor. Researcher have used organic field effect transistor along with electrolyte gate (EGOFET) as a biosensor [126]. One of the main challenge to develop EGOFET as a biosensor is electrochemical doping of ions from electrolyte into semiconductor, which results in decrease in capacitance and semiconductor electrical property. Thus, performance of EGOFET decreases drastically upon use. Incorporation of polymer gel matrix in EGOFET, may solve this problems and gives a definitive direction. Thus, in future, electrolyte based FET can be used as a bio sensor in various application such as cancer cell detection.

Device #	**Mobility ($cm^2 V^{-1} s^{-1}$)**	**Specific Laser Power (W)**	**R (AW^{-1})**	**EQE (%)**	**Response time (μs)**	**Detectivity D*(Jones)**
Device I	36.89	6.3×10^{-8}	32.5	6136	7.5	1.29×10^{12}
Device II	24.57	4.9×10^{-8}	8.98	1695	8.6	3.04×10^{11}
Device III	--	3.3×10^{-8}	17.52	3308	20.8	1.51×10^{11}
Device IV	14.8	2.7×10^{-8}	13.67	2582	--	--

Table 5.2: Key parameters and optical properties of $CuIn_7Se_{11}$ devices on SiO_2 thickness = 300 nm, V_d = 0.2 V, V_g = 0 V, λ_{laser} = 658 nm are listed.

Further, as fabricated FETs were used as phototransistor and opto-electronics properties are summarized here. Nearly pure photoconductive effect at negative gate voltage ($\gamma \rightarrow 1$) and photogating dominated photoconductive effect at positive gate voltage ($\gamma < 1$) was observed, indicating gate voltage controlled photocurrent generation mechanisms of photoconduction and it is further confirmed by time-dependent photocurrent. Several parameters corresponding to photodetectors such as responsivity, $R \approx 60.6$ A W^{-1}, EQE of the order 10^4 %, response time, τ_{90-}

$_{10}$ ~ 8.6 µs, characteristics response time $\tau_{3dB} \approx 2.17$ µs, bandwidth, $f_{3dB} \approx 73.4$ kHz, noise equivalent power, NEP ≈ 1.06 * 10^{-15} W $Hz^{-1/2}$ and specific detectivity, D* ≈ 3.15 * 10^{12} Jones were estimated. This parameters can be further tuned by application of gate voltage and drain voltage. Some of the key parameters of phototransistors that were investigated are summarized in table 5.2. Response time of $CuIn_7Se_{11}$ phototransistor (τ_{90-10} ~ 8.6 µs,) is comparable with response time of SnS_2 photodetector where $\tau_{on/off}$ ~ 5 µs, [49] which is fastest response among 2D materials currently reported and several orders of magnitude faster than previously reported group III-VI layered materials. Thus making $CuIn_7Se_{11}$ phototransistor one of the fastest photodetector among 2D materials based photodetector.

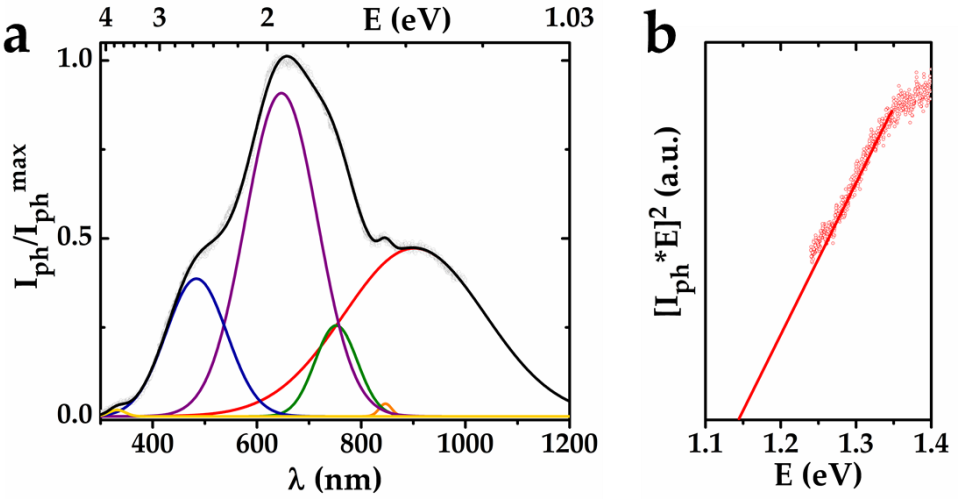

Figure 5.2: Photocurrent spectroscopy of CuIn7Se11 phototransistor. a) Photocurrent spectra consisted of multiple peaks. b) $(I_{ph} * E)^2$ *vs* E plotted which will be used to determine direct band gap energy.

Understanding of the spectral response of photodetector is important from fundamental as well as technical point of view. Photocurrent spectroscopy (PCS) is a follows similar fundamental theory as absorption spectroscopy. Thus using PCS for spectral response will not compromise any fundamental aspect, however advantage of using PCS is that it give spectral response in device mode. Thus, while developing a photodetectors for an industrial purpose, PCS

will come in handy. We have looked at photocurrent spectroscopy of $CuIn_7Se_{11}$ phototransistor and it is shown in figure 5.2a. It can be seen that multiple peaks are detected photocurrent spectra and we are in process of understanding this peaks. Peak at lower energy can be associated with band to band transition at band gap of material (shown by red curve). We have used relation between absorption and intrinsic optical transition along with fact that photocurrent is proportional to absorption and obtained a relation between photocurrent, I_{ph} and energy of excitation, E as $(I_{ph} * E)^2 \propto (E - E_g)$, where E_g is a direct band gap energy. Thus $(I_{ph} * E)^2$ *vs* E is plotted in figure 5.2b and x-intercept is direct band gap energy, E_g. We found direct band gap energy E_g, to be $\approx$ 1.15 eV. A further investigation are being carried out and this will be another project to start with during initial period of Ph.D.

Experiments shown through this thesis are carried out at room temperature. It will be interesting to see how electronic and optoelectronic transport behaves at lower temperature. As temperature is source of thermal energy for electron and by lowering temperature it is expected that electron will freeze, thus conductivity of semiconductor decrease at lower temperatures. Various interesting experiments can be carried out towards understanding some of fundamental properties of semiconductor. For example, low temperature electrical transport can be used to determine nature of electronic states in semiconductor [127]. Variation of band gap at lower temperature can manifest electron-electron, electron-phonon interactions in semiconductor [128]. Temperature dependent photocurrent can lead to determination of nature of traps states [120]. Thus, during initial period of Ph.D., I will spend time in investigating low-temperature electronic and opto-electronic properties of $CuIn_7Se_{11}$ FETs.

Due to exciting properties $CuIn_7Se_{11}$, in particular fast response time, it is expected that 2D forms other ternary systems like Lead Gallium Selenide ($PbGa_2Se_4$), Thallium Gallium

Selenide ($TlGaSe_2$) and Thallium Gallium Sulfide ($TlGaS_2$) will have similar properties. In particular, Lead Gallium Selenide in its bulk form are used as high electron mobility gamma-ray detectors, photodetectors, and sensors. It has indirect band gap of 2.3 eV and direct gap of 2.35 eV. Although properties at few layers are yet to be investigates, it is a promising material due to its properties at bulk. Thallium Gallium Selenide and Thallium Gallium Sulfide have relatively higher band gap of 1.95 eV and 2.45 eV, respectively, thus making them a promising materials for photocurrent spectroscopy as currently our experiments are limited within range of 1.2 eV and 4 eV. We have purchased $PbGa_2Se_4$, $TlGaSe_2$, and $TlGaS_2$ from 2Dsemiconductors, [129] a company which synthesizes layered materials in the bulk and monolayer form. We have purchased single crystal of above material and few layers can be exfoliated mechanically using scotch tape assisted exfoliation. Preliminary experiments like mechanical exfoliation and fabrication of device have been started and soon this materials will be our main focus.

After an extensive research that has been carried out in binary transition metal dichalcogenide, TMDs, like MoS_2, WS_2, $MoSe_2$, WSe_2, $MoTe_2$ etc., researchers are have shifted their interest towards synthesis of their alloys. In particular, molybdenum tungsten diselenide alloys ($Mo_{1-x}W_xSe_2$, $0 \leq x \leq 1$) [130] and molybdenum tungsten disulfide ($Mo_xW_{1-x}S_2$) [54] were shown to have some interesting properties, though extensive investigation of electronic and opto-electronic properties of this alloys is still unavailable. One of direction going into future would be investigate electronic and opto-electronic properties of $Mo_xW_{1-x}S_2$, which were synthesized at our collaborators, Prof. Terrones's lab at The Pennsylvania State University [54].

A high-electron-mobility transistor (HEMT) is another architecture of a FET where heterostructure of two materials with different band gaps is used as the channel instead of single channel semiconductor. HEMT was invented in 1979 by a Japanese researcher, Takashi Mimura

[131]. Most commonly used materials are GaAs and AlGaAs. At junction of two materials, due to band gap mismatch, conduction and valence band beds in order to match fermi levels. Thus at junction of two materials, electron are accumulated due to valley in conduction, forming two-dimensional electron gas (2DEG). The accumulation of electrons leads to a very high current as well as good performance of transistor. Although HEMT concept is very old, heterostructures based on 2D materials have gained attention in recent years and it is anticipated that heterostructures would be a next generation for 2D materials. Thus in future, my interested lies in synthesizing heterostructure and investigating their electronic and opto-electronic properties.

Template-assisted electrodeposition is one of traditional and strong technique to form nanostructured materials in one dimensional (1D). Group III-VI based 1D nanostructured materials can be easily synthesized from template-assisted electrodeposition and it will be interesting to see some of their properties [132]. Template-assisted electrodeposition is one of the simple technique to synthesis nanostructures and their heterostructure. Due to its simplicity, I would be able to mentor undergraduate or high-school student in synthesizing 1D Group III-VI materials based nanostructured and their heterostructure. This project can serve as mentoring experience for me as well as supplementary work toward my Ph.D. dissertation.

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APPENDICES

Two-dimensional materials and their prospects in transistor electronics

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Investigation of Electronic and Opto-electronic Properties of Two-dimensional Layers (2D) of Copper Indium Selenide Field Effect Transistors

Major Professor: Prof. Saikat Talapatra

Publications:

- Peer Reviewed Articles
  1. **P. D. Patil***, S. Ghosh*, M. Wasala*, S. Lei, R. Vajtai, P. M. Ajayan, S. Talapatra, "Electric Double Layer Field Effect Transistors using Atomically Thin Layers of Copper Indium Selenide ($CuIn_7Se_{11}$)", manuscript under preparation, 2017. *equally contributing authors.

2. S. Ghosh*, **P. D. Patil***, M. Wasala*, S. Lei, A. Nolander, S. Pooplasingam, R. Vajtai, P. M. Ajayan, S. Talapatra, "Fast Photoresponse and High Detectivity in Copper Indium Selenide ($CuIn_7Se_{11}$) Phototransistors", manuscript under review in ACS Applied Materials & Interfaces, 2017. *equally contributing authors.
3. P. V. Sarma, **P. D. Patil**, P. K. Barman, R. N. Kini, M. M. Shaijumon, "Controllable Growth of Few-layer Spiral WS_2", RSC Adv. **6**, 376 (2016); **DOI**:10.1039/C5RA23020A.

- Conference Proceedings/Abstracts
  1. **P. D. Patil**, S. Ghosh, M. Wasala, S. Lei, R. Vajtai, P. M. Ajayan, S. Talapatra, "Fast Photo-detection in Phototransistors based on Group III-VI Layered Materials", - APS March Meeting, New Orleans, LA, 2017. **Abstract**: K31.00012. (*Oral Presentation*).
  2. M. Wasala, **P. D. Patil**, S. Ghosh, S. Lei, R. Vajtai, P. M. Ajayan, S. Talapatra, "Temperature Dependent Photocurrent Spectroscopy of Few Layer $CuIn_7Se_{11}$", - APS March Meeting, New Orleans, LA, 2017. **Abstract**: H33.00011.
  3. S. Ghosh, M. Wasala, **P. D. Patil**, S. Lei, R. Vajtai, P. M. Ajayan, S. Talapatra, "Electronic Transport and Photo-Current Generation in Few Layer n-Type CuInSe Field Effect Transistor", - MRS Spring Meeting, Phoenix, AZ, 2016. **Abstract**: EP10.2.09.
  4. **P. D. Patil**, S. Ghosh, M. Wasala, S. Lei, R. Vajtai, P. M. Ajayan, S. Talapatra, "Electric Double Layer Field Effect Transistors using Atomically Thin Layers of Copper Indium Selenide (CuInSe)", - APS March Meeting, Baltimore, MD, 2016. **Abstract**: P16.00015. (*Oral Presentation*).