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TECHNIQUES FOR DIGITAL LOW DROPOUT REGULATOR MODELING AND TRANSIENT RESPONSE ENHANCEMENT

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by

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A Thesis
Submitted in Partial Fulfillment of the Requirements for the
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TITLE: TECHNIQUES FOR DIGITAL LOW DROPOUT REGULATOR MODELING

AND TRANSIENT RESPONSE ENHANCEMENT

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Low dropout regulators (LDOs) are important components for power management in modern integrated circuits. With the continued scaling down of power supply voltage, digital LDOs have become a more attractive design choice since they avoid the difficulty of designing high-gain amplifiers with low voltage. This thesis investigates techniques for both modeling and enhancement of digital LDO transient response. It discusses the importance of the equivalent series resistance at the output of an LDO, and proposes a simulation model for examining LDO transient response. In addition, the thesis studies circuit techniques to improve LDO transient response. Different LDO circuits are implemented and compared in this study.

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CHAPTER 1

INTRODUCTION

Power management has become an important issue in modern VLSI design due to the wide adoption of fine-grained power management in microprocessor and system-on-chips. These management schemes include both allocating function units to different voltage domains statically, as well as dynamic adjustment of power supply voltage and operating frequency according to throughput requirements. Low dropout (LDO) voltage regulators are often used to generate the desired voltage levels in these schemes due to their low noise and high power supply ripple rejection advantages.

Among the various LDO implementations, digital LDOs enjoy increased popularity. Analog LDO implementations utilize high-gain amplifiers, which are difficult to design with deep sub-micron CMOS technologies and low supply voltage. Digital LDOs eliminate the need for amplifiers, which has led to an increased research interest in digital LDO implementations. Several digital LDO designs have been presented over the past several years. These implementations can broadly be broken down into designs that utilize a comparator to detect the difference between the output and the reference level, and those that translate such voltage difference into other information. The former are discrete time circuits and use arrays of PMOS transistors as the power device, while the latter adjust the voltage at the gate of the power device to control the output voltage.

It is desirable to have fast and accurate response to large transient changes at load current or input voltage. This motivated significant research efforts on methods to

predict the transient response to such changes as well as techniques to improve the

LDO transient response. However, the existing models only consider system open loop

behavior.

In this thesis, multiple techniques for both modeling and improvement of

response for digital LDOs are examined. The rest of the thesis is organized as follows.

Chapter 2 provides a brief review of digital LDOs that are related to this study. Two

LDO circuit techniques are presented in Chapters 3 and 4 with the aim of improving

transient response. Chapter 5, then, presents the proposed simulation models of digital

LDOs. Finally, conclusions are provided in Chapter 6.

CHAPTER 2

LITERATURE REVIEW

Section 2.1 Review of PLL Based Digital LDOs

Phase-locked-loop (PLL) based implementations of digital LDOs have been presented in [1] and [2]. The two use different numbers of stages and different methodologies for the implementation of the PLL. Both, however, share the same design philosophy. Both utilize voltage-controlled oscillators to convert voltage difference to phase difference, where they differ is in the exact implementation [1, 2]. This type of circuit uses the phase difference to control a current to pull up or down the voltage at the gate of the output transistor [1, 2].

The circuit in [1] utilizes the output and reference voltages to create the currents for two oscillators made up of three delay cells each. The output of these two oscillators drives a phase-frequency detector, which converts the phase difference between the two to a digital signal [1]. This allows the circuit in [1] to convert the difference in voltage to a digital control signal without using a comparator, as it converts the voltages to a current then to time then compares the times and uses that to produce a digital signal. The design claims the advantage of not requiring an off-chip capacitor, which is generally required in other designs [1]. The paper presents a transfer function for the output of the circuit, which is

$$T(s) \cong A_{OL} * \frac{\left(1 + \frac{s}{\omega_z}\right)}{s^2} \tag{1}$$

where A_{OL} is the open loop gain, and ω_z is the zero frequency [1]. This shows that if no output capacitor is considered, an LDO system has two-poles at a frequency of 0 Hz.

The zero in the equation was introduced as a design choice by [1] and is not inherent to a digital LDO system. This indicates that it was necessary for the stability of the system after removing the output capacitor.

The circuit in [2] features an adjustable number of stages. Unlike [1], the PLLs in [2] are used as voltage-controlled oscillators. The adjustable number of stages are either 13 or 25, and the 12 additional stages are used to choose between high frequency and low frequency operation [2]. The digital control differs as well with a 32-bit Johnson Counter used instead of a phase-frequency detector and the VCO outputs used as clock signals for the counter [2]. An advantage is claimed from this digital logic being able to run at a power supply lower than either the reference, output or power supply for the output yet still control the output digitally in order to reduce the overall power consumption [2]. Unlike [1], an output capacitor is utilized in [2] and no zero is introduced. The paper includes a Bode plot indicating that with the capacitor chosen the second pole position is around two gigaradians per second at a low current and a teraradian per second at high load [2]. The Bode plot shows that with the capacitor chosen the second pole is moved beyond the unity gain frequency in order to stabilize the system [2]. The claimed phase margin is in excess of 80 degrees for both situations, indicating that the second pole was pushed sufficiently far to be ignored [2]. This indicates that differing loads will change the stability of an LDO circuit by moving the second pole.

Section 2.2 Review of Comparator-Based Designs and Modeling

Multiple comparator-based digital low dropout regulator designs have been presented over the past few years. A generic block diagram for such designs is presented in [3]. This is reproduced below.
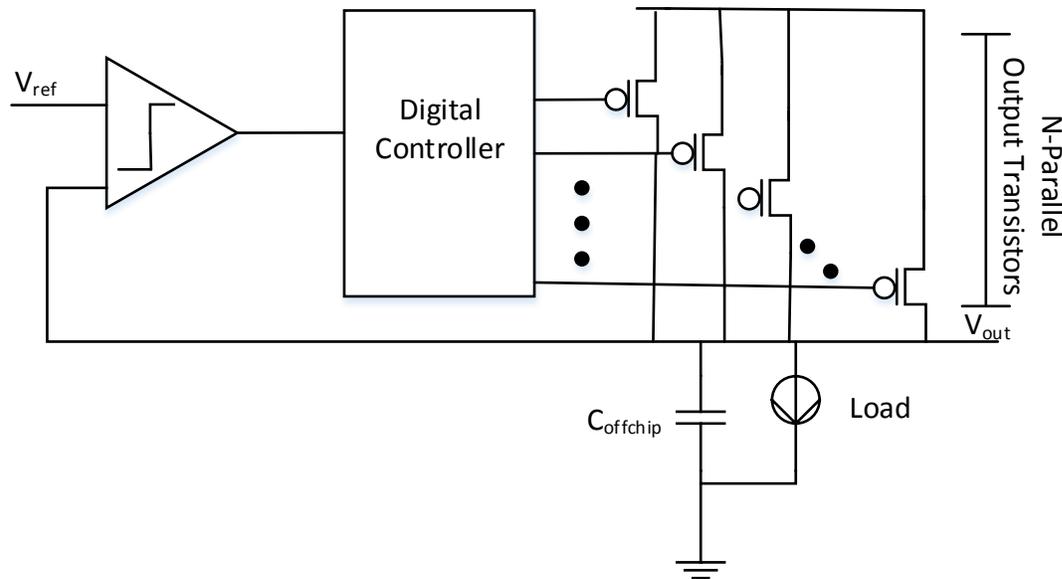
Figure 1 Block Diagram of a Comparator Based D-LDO [3]

As can be seen these designs utilize a comparator to determine whether the output is too high or too low then use digital control to control the number of transistors that should be on. Unlike the circuits using PLLs, such as those presented in [1] and [2], this type of circuit requires a clock signal to operate, as the comparator and control logic will be discrete time systems [3]. An off-chip decoupling capacitor is typically connected to the LDO output node. Some designs use multiple comparators to monitor whether large changes have occurred by having additional comparators monitor voltages offset from the reference, which will generate multiple inputs to the digital logic [4-6].

The design in [3] uses a simple bi-directional shift register to accomplish this control. This shift register uses D-flip flops and multiplexers with thermometer

encoding. In order to ensure the thermometer code is given it initially sets all of the D-flip flops to a value of 1 in order to turn all transistors off, which allows the circuit to start consistently [3].

Recent designs have taken approaches to improve the response to changes in operating conditions. These have primarily been concentrated on changing the digital control logic in response to a sudden change in circuit conditions [4-6]. Three different methods for this will now be reviewed. The circuit in [4] utilizes an up/down counter to control the output of the circuit with 9-bits. It uses 511 transistors with each counter output driving the number of transistors associated with it [4]. For faster response, the circuit includes a transient mode detector, which detects if the circuit has entered a state that is too far away from the reference and subsequently generates a signal that makes the circuit count four times as fast [4]. This is accomplished by using a cyclic time delay circuit (TDC) to generate the clock for the up/down counter, while using an exterior clock to both control when the TDC is operational as well as the comparators [4]. In addition to the aforementioned circuit techniques, [4] presents an open loop S-domain model for the stability of a digital LDO. This model assumes knowledge of the overall gain of the circuit, the load conditions, transistor characteristics and clock frequency [4]. The transfer function is as follows:

(2)

$$T(s) = H_0 \frac{e^{-s/f_{clk}}}{s} \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

where H_0 is the open loop gain of the circuit, ω_z is the zero frequency, ω_p is the pole frequency, and f_{clk} is the clock frequency [4]. Unlike the model in [1], it includes an exponential term and a pole with non-zero frequency. The latter is due to the off-chip capacitor being included, while the former comes from the zero order hold at the

counter output [4]. The zero in this model comes from the equivalent series resistor of the output capacitor [4].

The circuit in [5] uses multiple methods to improve its response as well as its steady-state effect and power consumption. Similar to [3], [5]uses a bi-directional barrel shifter to control the output, and as such turns on or off transistors in a thermometer coded order. One of the methodologies used for detecting large changes in circuit parameters is similar to the use of the TDC in [4], in that it causes the circuit to turn on or off multiple transistors per clock cycle [5]. [5], however, implements this faster switching by using 4-1 multiplexers to switch a variable number of transistors at the same time within the shifter. Additionally, for large load changes the circuit's clock frequency is vastly increased to around 400 MHz. According to the paper, this renders the circuit marginally stable and switches transistors rapidly [5]. To improve its steady state and response to small changes in circuit conditions, the circuit relies on knowledge about the state of the load and uses different clock speeds depending on load conditions [5]. [5] determines this by checking whether the number of conducting transistors is in the first, middle or last third of the array. This was primarily shown to have improved current efficiency by [5].

As mentioned, [5] relies on knowledge of the effect of various changes on the transfer function of the LDO. [5] presents an open loop Z-domain model for the stability of a digital LDO and uses it to explain the reasoning behind the previously discussed changes. This model assumes knowledge of the analog DC gain, digital gain, load conditions and clock speed of the circuit [5]. The equation given is:

(3)

$$T(s) \cong \frac{K_{Barrel}K_{DC}z^{0.5}}{(z-1)\left(z - e^{-F_{LOAD}/F_{CLK}}\right)}$$

where F_{CLK} is the clock frequency, F_{LOAD} is the position of the pole due to the load, K_{Barrel} is the digital gain, and K_{DC} is the DC gain of the output stage [5]. It may be noted that this and the S-domain model are not a perfect match; however, this can be concluded to be due to the difference between the delays through the circuit. Since the half clock cycle delay is modeled in the latter circuit inputs, a $z^{-0.5}$ is introduced into the transfer function. The $e^{-s/f_{clk}}$ converts to z in the z-domain, resulting in a net term of $z^{0.5}$. The lack of the zero, on the other hand, occurs because [5] does not consider the equivalent series resistance of the off-chip capacitor, while [4] does. Whether this is important and if including a resistor can help the output characteristics will be examined later. The circuit parameters modeled are also discussed by [5]. The most significant among these is the F_{LOAD}/F_{CLK} relation, which is shown to decide whether the circuit would show overdamped or underdamped behavior, with a low ratio giving an underdamped response and a high ratio giving an overdamped response [5].

The design in [6] introduces a fast current tracking scheme with three different techniques to respond to changes in load. Two of these are triggered by a detection of a large load change, while the third activates at every crossover of the reference voltage by the output [6]. The third technique takes the two previous crossovers' states and averages them then changes the output state to that average [6]. The averaging is proposed to remove the ringing after a change by immediately finding the correct state for the circuit conditions [6]. The justification in [6] assumes a perfect sine wave behavior of the output voltage before and after the transition with simply a larger or

smaller magnitude depending on circuit conditions and thus the number of transistors over or under the correct value at each crossover is equal [6]. Since the second crossover would have precisely the opposite error as the first, the average then gives the correct value [6]. The other two techniques are responses to a detected droop or overshoot, which is found by two additional comparators that monitor for those [6]. In response to a detected droop the circuit in [6] acts much the same as [4] and [5], turning on multiple transistors at a time to speed the response. However, when an overshoot is detected the circuit drops the state to 0 [6]. This is explained to cause the output to immediately begin dropping as it causes the circuit to conduct no current at all, causing all current to come from either the off-chip capacitor or leakage [6]. This is then held; due to the main comparator still saying the voltage is too high, until the next crossover where averaging once again commences [6].

CHAPTER 3

DESIGN OF DIGITAL LDO CIRCUIT

In this chapter, a comparator based digital LDO circuit is developed using a 130 nm CMOS technology. The design follows the scheme in [3] and will be used as a reference design to compare with model estimation and improved LDO design in the following chapters. In addition, the developed circuit is simulated in this chapter to investigate the effect of equivalent series resistor (ESR) of the output capacitor on the digital LDO output response. Finally, a proposed design technique to add an analog feedback loop in the digital LDO circuit is examined. The schematic of the developed LDO is shown in Figure 2, where each n is a one-bit digital controller that outputs a binary value Q to control a single transistor. There are 256 control blocks making up a 256-bit bi-directional shift register. The design of its functional blocks are discussed in the following sub sections.
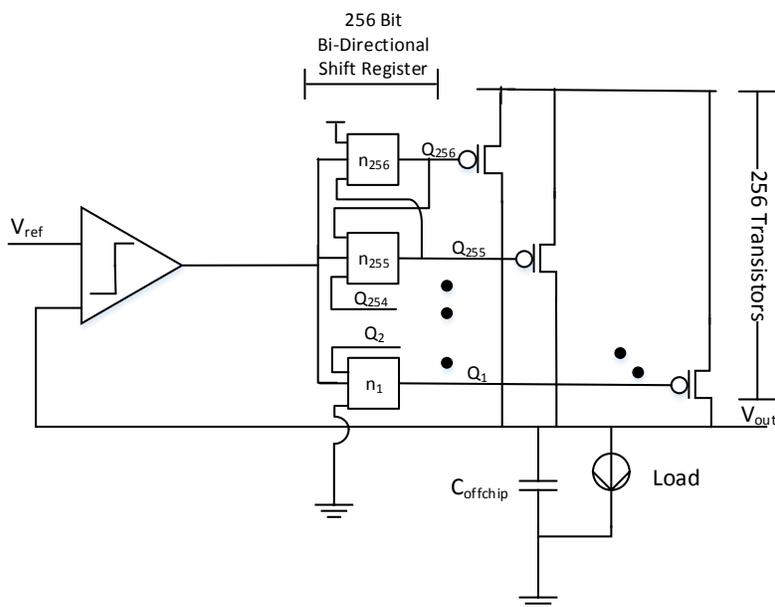
Figure 2 Reference Digital LDO Schematic

Section 3.1 Design Considerations and Implementation

The comparator is used to compare the output with a reference voltage to produce a one-bit digital output. The accuracy of this circuit directly affects the precision of the LDO circuit. The comparator used in the reference design is shown below [3].
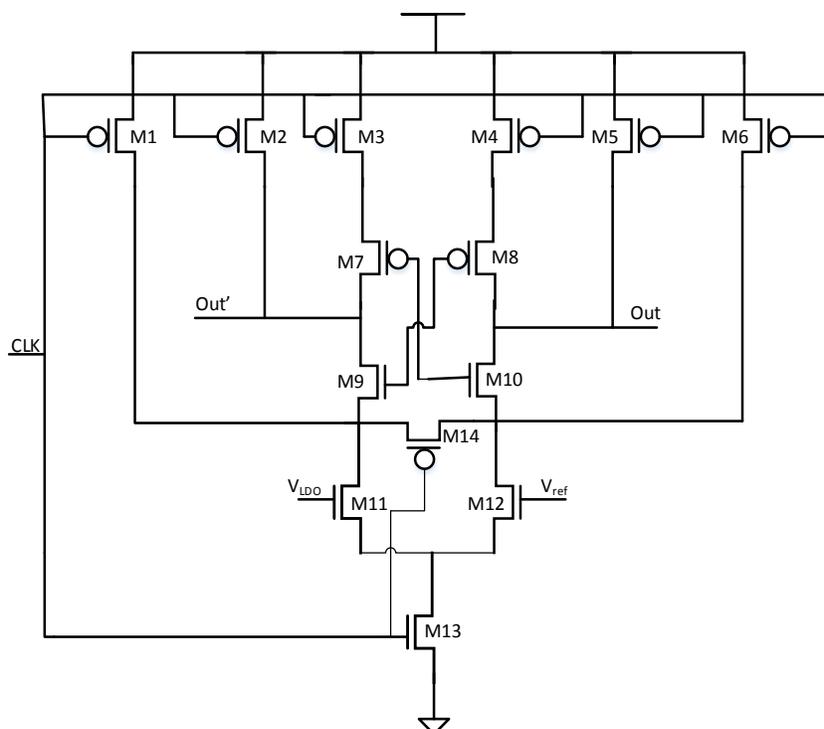
Figure 3 Comparator used in [3]

It has pull-up transistors, M1-M6, to pull up every line evenly during the precharge phase, which is when the clock signal is low. This is in addition to an equalization transistor, M14. To search the optimal transistor sizes for the design two circuits, one with transistor widths of 2.4μm for the PMOS and 1.2μm for the NMOS, and the other with transistor widths of 320nm for the PMOS and 160nm for the NMOS are created. In both designs, the transistor channel length is 120 nm. The two circuits are simulated with a supply voltage of 0.5 V. Simulation shows the design with larger transistor size is

actually slower than the design with smaller transistor size. This is mainly due to the

large parasitic capacitance caused by the large transistor size. Thus, the design with

smaller transistor size is used.

It is noted that this design utilizes both equalization and pull-up devices for

making the nodes to reach the same voltage during the precharge phase. To test

whether both are necessary the equalization transistor is removed resulting in the

following schematic.
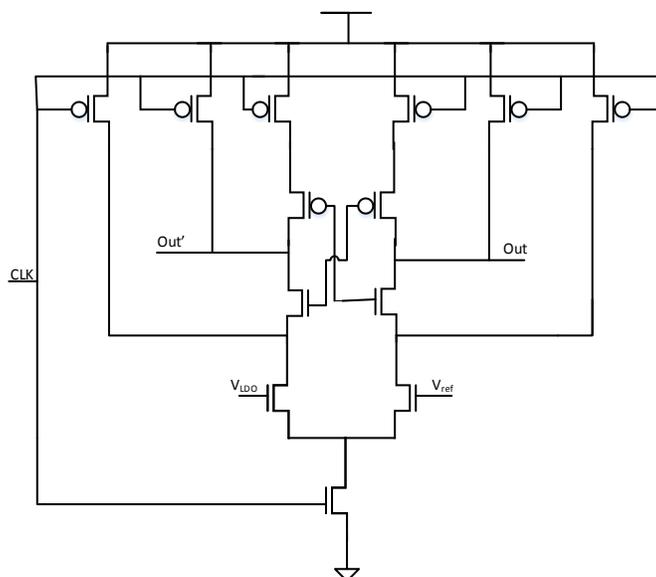
Figure 4 Comparator without Equalization

This new design relies entirely on the pull-up transistors during the precharge phase.

The circuit was simulated and found to work just as well to equalize the two output

nodes. Thus, the comparator without equalization and with the small transistor size is

used in the LDO design. To ensure the same capacitive load is present at both output

nodes, two inverters are added to isolate the comparator output nodes from the rest of

the circuit.

Sizing of the output transistors is also critical as this significantly affects several parameters of the digital LDO. The most important of these is the maximum output current for a given power supply and output voltage drop. Additionally, a larger transistor size creates a larger ripple with faster startup as each transistor conducts a larger amount of current, potentially. In theory, a number of transistors in parallel with the same length should be equivalent to a single transistor with a width equal to the total of the transistors in parallel. Thus, to find the minimum size, a single transistor's width was parametrically analyzed with steps of 160nm. For the design target of V_{dd}=0.5 V, V_{out}=450 mV and $I_{out,max}$=200 μA, the minimum transistor width is between 64.16 and 64.32 μm. Since the number of transistors in the reference is 256, the 64.16 μm width is then divided by 256 to find the size per transistor then rounded up to nearest practical value, which is 280 nm.

To ensure functionality, the width of these transistors is tested with a more practical setup as shown below.
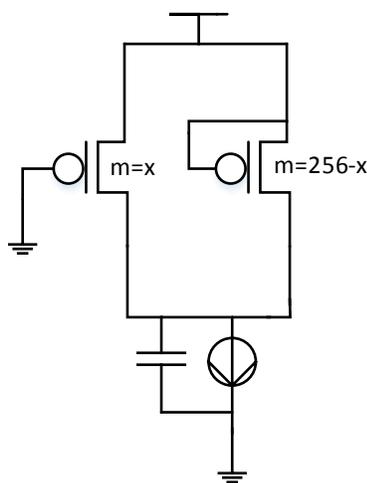
Figure 5 Transistor Number Testing

This test allows the number of transistors being on to be varied via multiplicity. It uses a variable x that sets the number of conducting transistors, and since the maximum

number of transistors is 256, the off-transistor number is 256-x. However, in this setup

even when all 256 transistors are on, the output voltage cannot reach 450 mV with

widths of 280 nm, 320 nm, and 360 nm. So 400 nm transistor width is chosen for the

final designs. This leads to a total width of 102.4 µm, or roughly double what is

expected from the first approach. The relation between the output voltage and the on

transistors is plotted. It is found that the number of on transistors is between 212 or 213

when the output voltage is close to 450 mV.
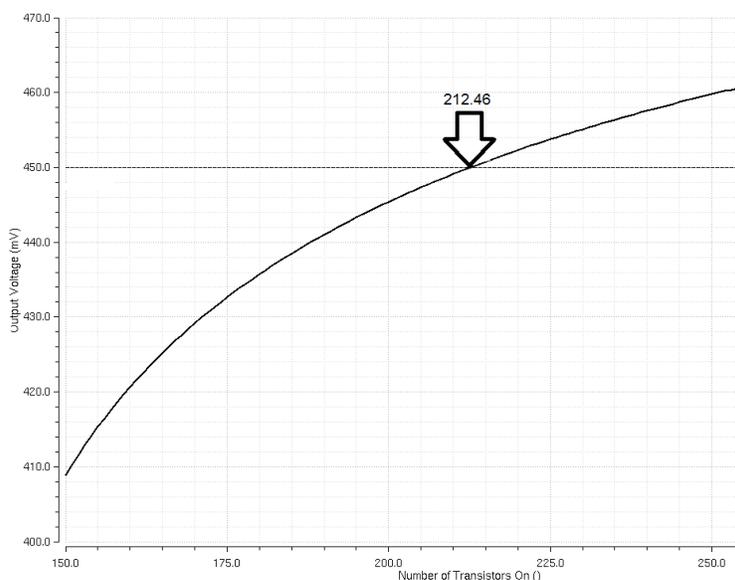
Figure 6 Voltage in Terms of Number of Transistors On

For the digital control of the output stage, the design uses a bi-directional shift

register [3]. In order to ensure proper encoding it is necessary to set a thermometer-

coded pattern into the shift register to remove the possibility of 1s or 0s being chosen

randomly during start-up, which could lead to unexpected problems during circuit

operation. As this is also to be used as the base shift register for the other design, it is

decided to implement the set control outside of the D-Flip flop. The schematic of the

unit block of the shift register is shown in Figure 7.
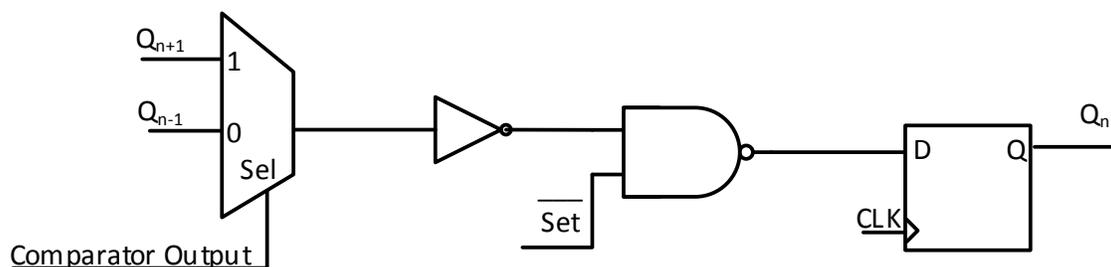
Figure 7 Shift Register Element

Section 3.2 Effect of Equivalent Series Resistor on D-LDO Transient Response

It is noted that the s-domain model considers a zero caused by the equivalent series resistor of the output capacitor, while the z-domain model ignores it [4-5]. To investigate the significance of the equivalent series resistor (ESR) various simulations are conducted using the developed reference LDO circuit with or without a resistor in series with its output capacitor. This is tested at the design target. Testing is done with resistances from one ohm to 1000 ohms scaling by orders of magnitude, as well as without any resistance, for comparison.

First, the startup is tested and the result is shown in Figure 8. The 1 Ω resistance has no obvious effect, while the 10 Ω and 100 Ω resistors appear to reduce the ripple with small effect on the peak. Additionally, with the largest resistance tested a significantly increase in start-up time is observed, though the peak is eliminated.
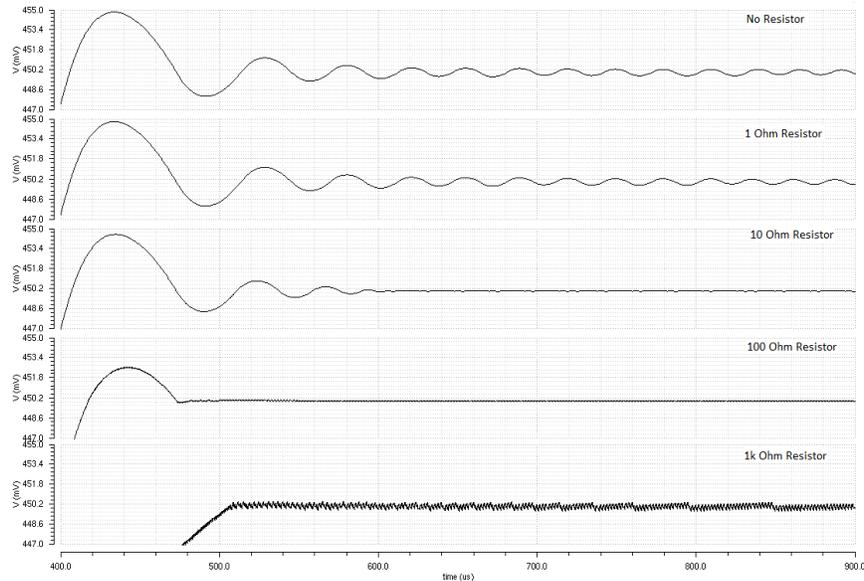
Figure 8 Startup with Differing Resistances

A significant difference in the ripple is noted in Figure 8. The plot is rescaled to form Figure 9, which examines the post-settling ripple. Looking at the ripple after settling it is observed that the addition of the 10 Ω resistor has the greatest effect on the settled ripple, as shown in Figure 9. Additionally, unlike the sinusoidal behavior at low resistances, higher resistances exhibit a square wave behavior.
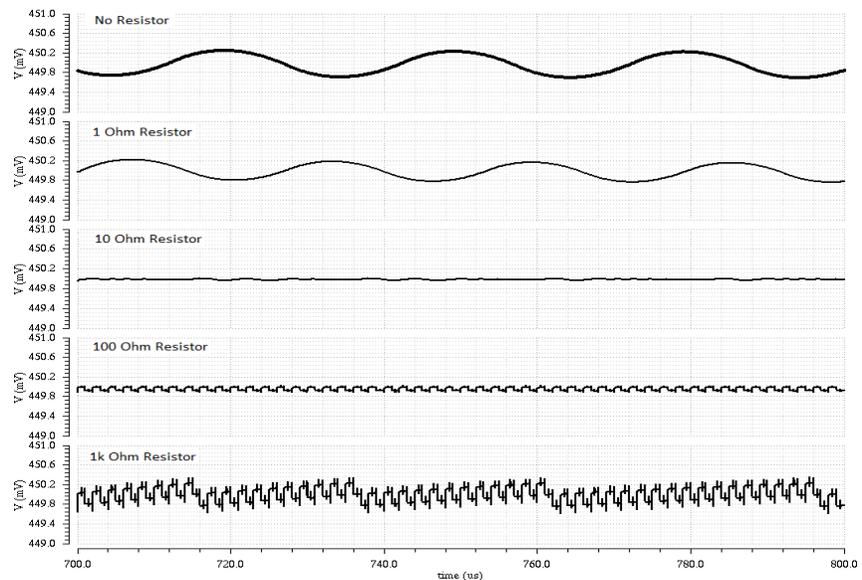
Figure 9 Steady State Waveforms with Different Resistances

Table 1: Effect of Different Resistor Sizes on Simulation Results

Resistance	Peak Time (us)	Peak (mV)	Ripple Maximum (mV)	Ripple Minimum (mV)	Overall (mV)	Ripple Improvement
0	434.01	454.81	450.26	449.688	0.572	-
1	434.01	454.77	450.193	449.753	0.44	23%
10	435.01	454.55	450.008	449.948	0.06	90%
100	442.01	452.68	450.025	449.858	0.167	71%
1000	520.01	450.43	450.355	449.571	0.784	-37%

The net effects are summarized in Table 1. As observed from Figure 9, the greatest effect on the ripple is produced by the 10 Ω resistor, while the 100 Ω resistor also has a very significant effect. The 1000 Ω resistor increases the ripple, which indicates that the sizes of resistances that have an improvement effect fall within a certain range. It is thought this range is between the clock frequency and the second pole position. The one Ω resistor places the zero above the clock frequency and has a far lesser effect, while the 1000 Ω resistor places the zero below the second pole frequency and has a negative effect on circuit performance.

Section 3.3 Analog Feedback Circuit

It is proposed to add an analog feedback loop into the output stage of a D-LDO circuit using capacitor feedback. The aim is to create a fast response by allowing the circuit to give an initial reaction without waiting for the next clock cycle. The capacitor would be placed between the control line and the output on each transistor to create a feedback path, as shown in Figure 10.
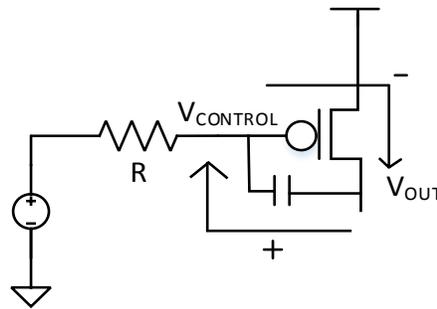
Figure 10 Capacitive Feedback

During steady state the capacitor has charge Q=C*(V_{OUT} - $V_{CONTROL}$). If V_{OUT} undergoes a rapid decrease or increase, then the $V_{CONTROL}$ line will be pulled with it either up or down, in order to keep Q constant. This will then cause each transistor to conduct more or less current than before, whichever is against the change at the circuit output. In theory, this should make the circuit more resistant to changes. However, this means the $V_{CONTROL}$ line cannot be strongly held or else the driver circuit will counteract the feedback. In other words, the R value in Figure 10 must be large.

To make the line voltage responsive to the capacitive feedback, it is necessary to weaken the transistors driving it. However, a weak driving circuit tends to be slow when charging signal values, which is undesirable. In order to avoid this problem, a pulse source and a weak inverter are used in the driver circuit. This circuit is designed to give a pulse to turn on the transistor when the state would normally change from off to on. No pulse source is utilized for changing the state of the transistor to off, since the number of conducting transistors control the output. The schematic of the driver circuit is shown in Figure 11.
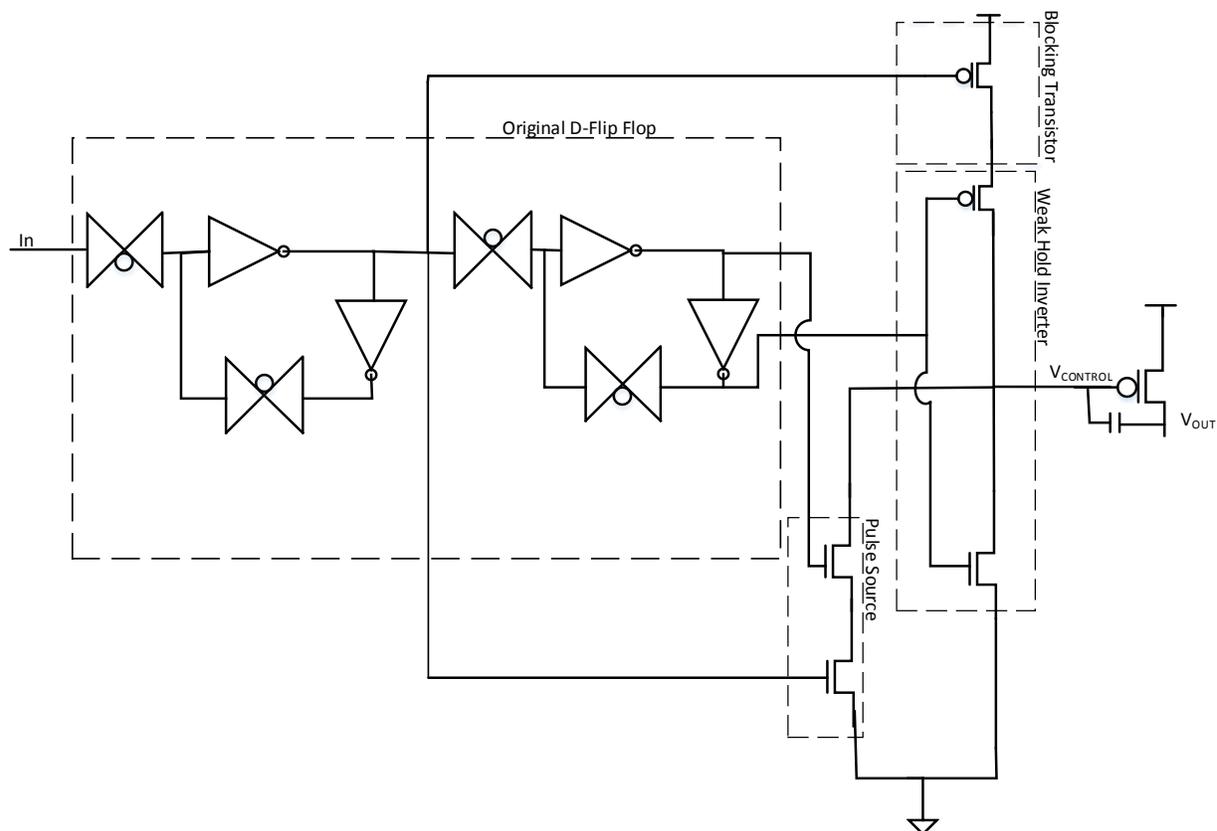
Figure 11 Final Design of Output Stage

It is found that this circuit's D flip-flop must be rising edge triggered in order to have the pulse circuit be active during the time when the comparator has a decision stored. The comparator is rising edge triggered, so the comparator will have the value between the time it makes its decision and the falling edge of the clock. In a rising edge triggered D flip-flop, the first pass transistor is active while the clock is 0. The pulse source will then act as falling edge triggered. This nets an odd effect due to the turning off process being rising edge-triggered and using the output of the D flip-flop. If one of the digital control bits is switched in consecutive clock cycles, the transistor will be off for one and a half clock cycles and on for only a half clock cycle. Since the pulse and output of the D flip-flop are triggered on opposite edges of each other, a PMOS transistor is added to prevent a Vdd to ground short when the pulse circuit is active by

blocking the hold inverter's Vdd connection. Additionally, the timing has to be carefully

planned to have the clock to the output line delayed until after the comparator result. If

the clock is not delayed adequately then the pulse circuit either activates on every

transistor in series, as each pulse source activates the next, during one clock cycle or

will not activate at all depending on the exact implementation of the rest of the circuit.

The output logic of the output stage circuit is described below.

Table 2: Logic of Pulse Source

Previous State	Next State	Control	Clock Edge
1	0	Pulse 0	Falling
1	1	Hold 1	N/A
0	0	Hold 0	N/A
0	1	Change to 1	Rising

Overall, this addition is expected to reduce the settling time, improve the regulation

characteristics, including peak and settling time, while increasing the power

consumption of the overall circuit minimally.

Section 3.4 Simulation Results

The developed LDO circuits are simulated to obtain their performance

parameters including load regulation, line regulation, power consumption, settling time,

peaking, and ripple size. The setup uses a 200 μA to 100 μA step for load regulation

and a 500 to 550 mV step for the line regulation simulation. The power supply voltage

is 0.5 V and clock frequency is 1 MHz in simulation. In addition, a 100 nF capacitor is

added to the output node. In some simulations, equivalent series resistance is added to

the output capacitor. For the LDO with the proposed capacitive feedback, the feedback

capacitor is 100 fF. These essential parameters used in the simulation setup are

summarized in Table 3.

Table 3: Setup Parameters

Component	Value
Load Capacitor	100 nF
Feedback Capacitor	100 fF
Series Resistor	10 Ω
Clock Frequency	1 MHz
Reference Voltage	450 mV
High Load Current	200 µA
Low Load Current	100 µA
High Power Supply	550 mV
Low Power Supply	500 mV

Section 3.4.1 Demonstration of Testing Methodology

Due to the existence of the ripple decisions have to be made about how to obtain

the values to be compared. This is explained with the plot shown below. As can be

seen there are four vertical lines, these denote the boundaries where averaging is

conducted for obtaining the output voltage. As can be seen, they describe two

complete cycles of the waveform in both states. This is thought to capture what the

actual average is, as the circuit is considered settled when it enters a repeating state.

The maximum and minimum of the ripple are measured during this time period as well.

Additionally, the settling time is taken at the first peak after the waveform entered its

final state.
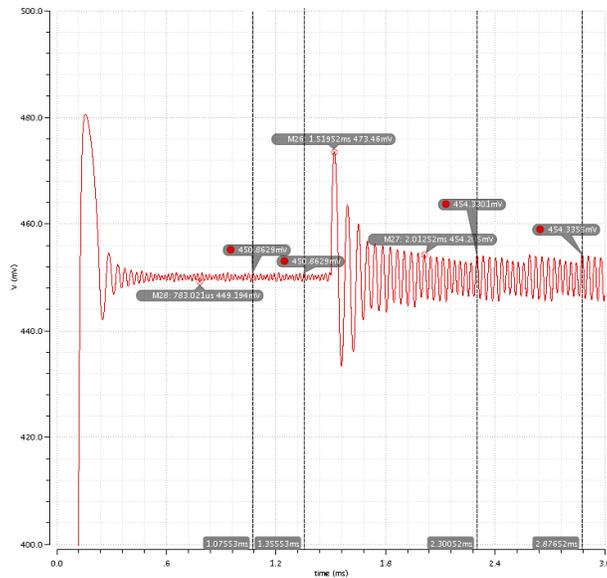
Figure 12 Demonstration of Testing Procedure

Section 3.4.2 Simulation without Output Resistor

Initially, simulations are conducted without considering ESR of the output capacitor. Figures 13 and 14 show the simulation results for line regulation and load regulation tests. The reference design is the circuit without the proposed capacitive feedback and the proposed design is the circuit with it.
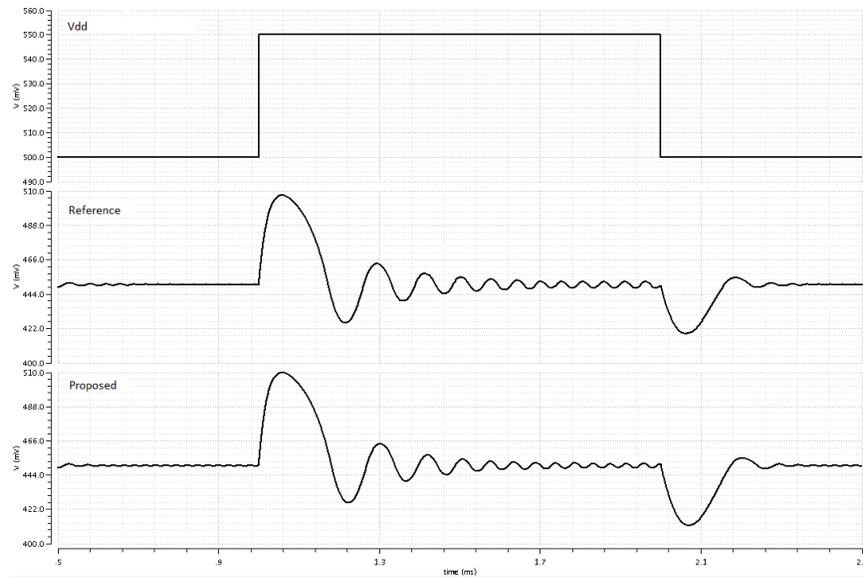
Figure 13 Line Regulation of Circuit with and without Analog Fast Loop
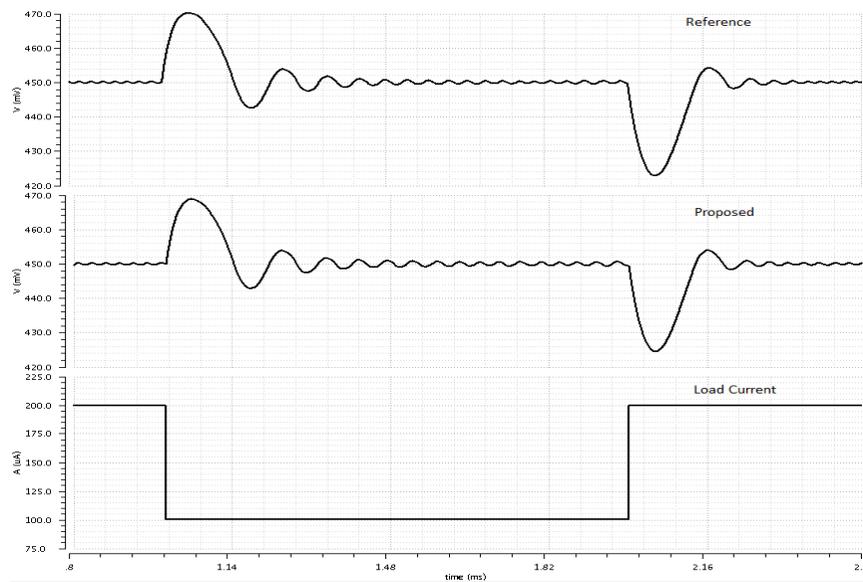
Figure 14 Load Regulation of Circuit with and without Analog Fast Loop

The difference is not readily obvious from these figures. The results are summarized into the tables below with the regulations split out from each other for ease of reading. Additionally, Table 6 summarizes the other parameters measured.

Table 4: Load Regulation Results for Simulation without Resistor

Parameter	Reference	Proposed	Improvement
Peak (mV)	468.9	470.5	-8.45%
Load Regulation (mV/mA)	0.18	0.13	27.86%
Settling Time (ms)	0.68	0.66	3.30%

Table 5: Line Regulation Results for Simulation without Resistor

Parameter	Reference	Proposed	Improvement
Peak (mV)	509.9	507.3	4.52%
Line Regulation (mV/V)	0.48	0.28	41.67%
Settling Time (ms)	0.70	0.79	-12.14%

Table 6: Other Measured Results for Simulation without Resistor

Parameter	Reference	Proposed	Improvement
Base Ripple (mV)	0.57	0.40	30.60%
High Power Supply Ripple (mV)	4.02	2.95	26.75%
Low Current Ripple (mV)	1.27	0.94	25.75%
Power Consumption (µW)	100.41	100.50	-0.09%

The above tables show the ripple and regulation have a pronounced improvement, while the peak voltage is slightly worse in the proposed LDO circuit. The proposed LDO circuit, also has a slightly larger power consumption overall.

Section 3.4.3 Simulation with Output Resistor

The two circuits are also simulated while considering a potential ESR of the output capacitor. The ESR value is set at 10 Ω in the simulation. The obtained results from line regulation and load regulation tests are shown below.
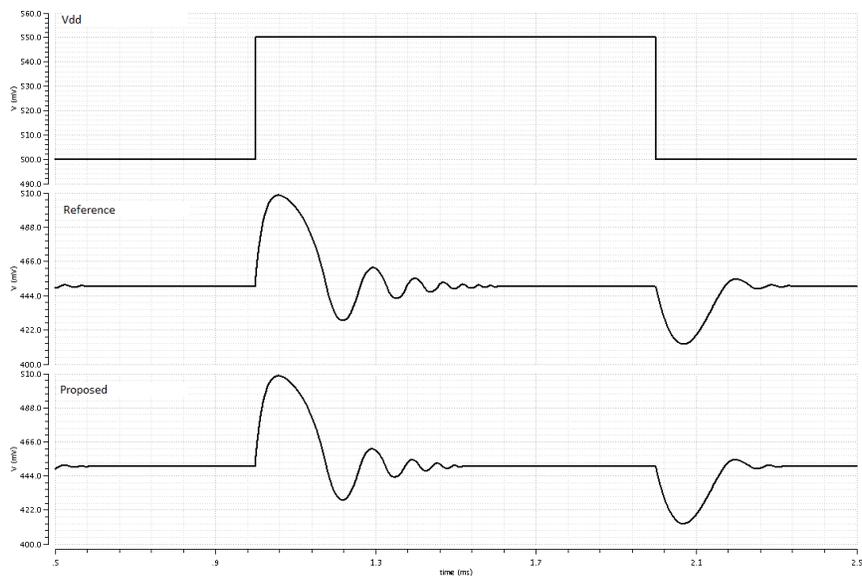
Figure 15 Line Regulation with Output Resistor
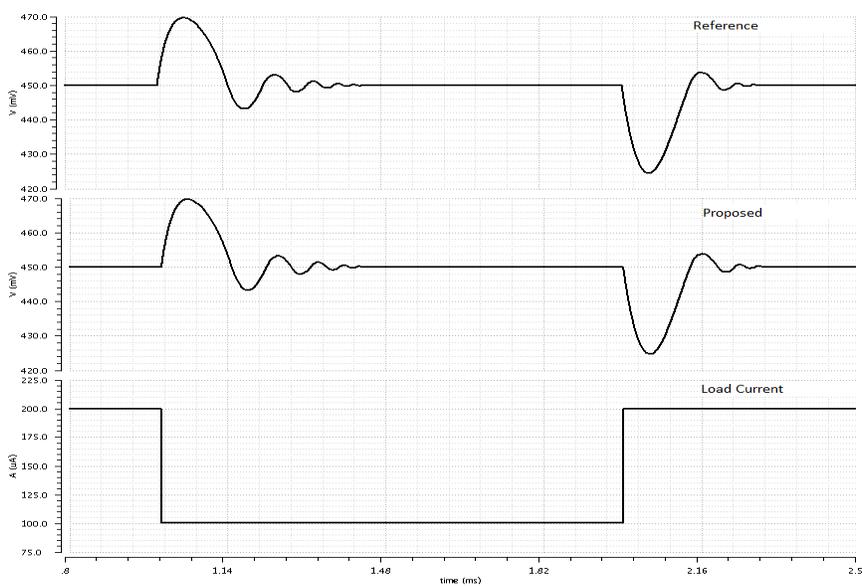
Figure 16 Load Regulation with Output Resistor Included

As before, data analysis is conducted in accordance with the procedure previously outlined. The obtained results are listed in the following tables. Power consumption is not included since it does not have a significant change from earlier tests.

Table 7: Load Regulation Results with Resistor Added

Parameter	Reference	Proposed	Improvement
Peak (mV)	469.7	469.7	-0.20%
Load Regulation (mV/mA)	0.035	0.030	14.37%
Settling Time (ms)	0.45	0.45	-1.25%

Table 8: Line Regulation Results with Resistor Added

Parameter	Reference	Proposed	Improvement
Peak (mV)	508.52	508.59	-0.11%
Line Regulation (mV/V)	0.10	0.28	-178.92%
Settling Time (ms)	0.65	0.53	18.18%

Table 9: Other Measured Results with Resistor Added

Parameter	Reference	Proposed	Improvement
Base Ripple (mV)	0.060	0.108	-79.80%
High Power Supply Ripple (mV)	0.104	0.166	-59.34%
Low Current Ripple (mV)	0.055	0.096	-73.34%

In this case, the proposed design is inferior nearly across the board with only load

regulation showing an improvement, but not as large as the previous result. All

parameters on both circuits, however, are improved from the previous test with the

ESR. This indicates the important role of ESR in achieving stable digital LDO output.
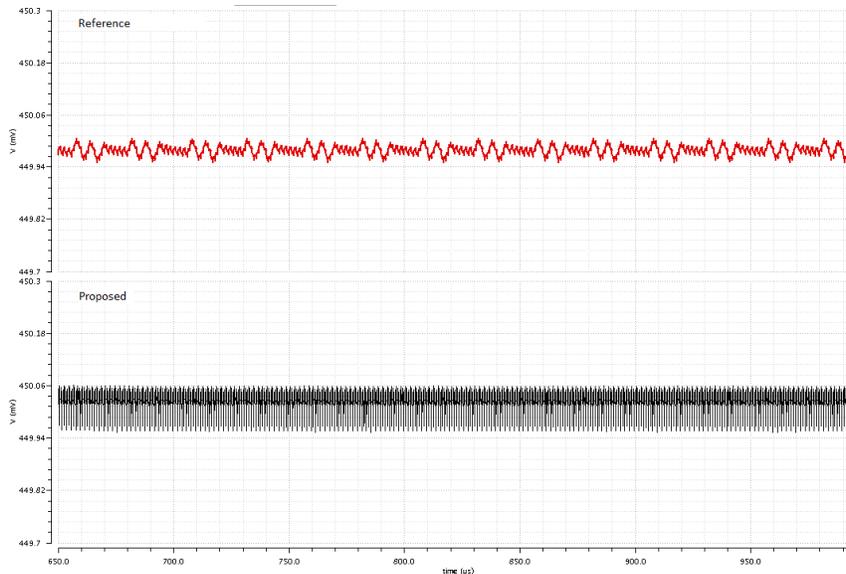
Figure 17 Ripple Patterns of Designs with Output Resistor Added

A close look at the LDO outputs is shown in Figure 17. As can be seen, the output of the reference design is a small repeating pattern, while the output of the proposed design seems to be spiking. This is found to be a case where at every clock edge a glitch would occur in the output of the proposed LDO circuit.

Section 3.4.4 Problems Inherent with Weakened Control Line

The glitch issue is initially thought to be an implementation issue and an attempt is made to fix it. However, removing the easily traceable glitches did not fix the output and remove the spikes. To test if this is inherent or a product of implementation, first, a simulation is run without the capacitor but with the weakened hold transistors and pulse source to check if this is due to the capacitor itself. This results in the ripple below.
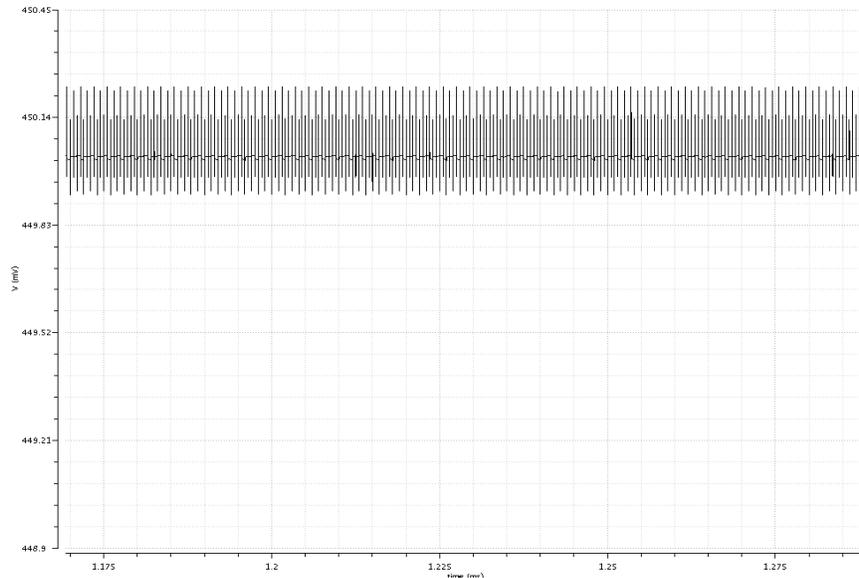
Figure 18 Ripple of Proposed Circuit without Feedback Capacitor

As can be seen, this exhibits a markedly similar behavior to the proposed circuit, though the glitches are larger in this case. The problem is thus with the weakening of the control line rather than the capacitor feedback, in fact, this suggests that the capacitor acts to minimize the effect on the output. When the clock edges were analyzed it is found that the largest glitch on the control line occurs one full clock cycle after a high-to-low transition on the control line but is merely six millivolts in size. Additionally, the glitch does not occur on every clock edge. The only glitch that seems to be a possible culprit by occurring on every clock edge is a five-millivolt glitch due to clock feedthrough. The effected line is an input to the pulse element, however, this should not have been important as only one of the input lines had a glitch and one line cannot generate a pulse. However, it illustrates how vulnerable this circuit is to even minor glitches. Due to this vulnerability, the circuit is deemed inappropriate for further study.

CHAPTER 4

LDO DESIGN WITH IMPROVED TRANSIENT RESPONSE

Various techniques have been proposed in literature to improve digital LDO

transient response. Among them, an interesting approach is performing moving

average calculation for the number of power transistors to be turned on [6]. The

implementation of this approach in [6] utilizes binary coding to control the number of

transistors on. Such an implementation is prone to transition glitches. To address this

problem, an improved implementation using thermometer coding is presented in this

chapter. An efficient binary code to thermometer code converting circuit is presented.

Also, this chapter provides a more comprehensive justification for the averaging

technique.

Section 4.1 Justification of Averaging Method

The ripple of the LDO output during its settling process is due to the mismatch

between the digital update rate and the pace of the output change. Because of the

large output capacitor, the output voltage change is typically slower than the digital code

update. As shown in Figure 19, when the output voltage becomes close to the target

voltage, the digital code in the circuit has already passed the target digital code.
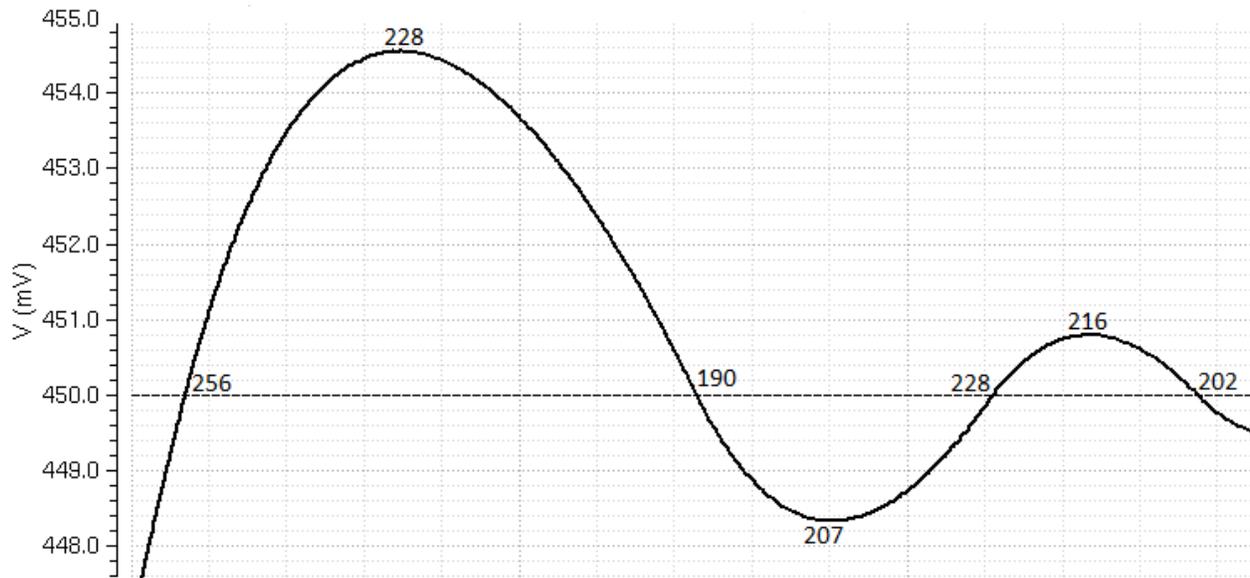
Figure 19 Number of Transistors at Peaks and Crossovers

The plot also shows that the codes at the peaks and valleys are roughly the average of the values at the adjacent crossing points. Additionally, the digital codes at the peak or valley positions are fairly close to the average of the surrounding settled digital values. This is shown in the following table comparing number of transistors at peak or valley with the average of the two points around it.

Table 10: Number of Transistors On

At Transition	256	190	228	202	222	206	219	208	217	210
Average		223	209	215	212	214	212.5	213.5	212.5	213.5
At Peak or Valley		228	207	216	210	215	210	215	211	212

Averaging can be further proved mathematically as a method to roughly find the code at the peak for all cases for a DLDO. This is explained using the LDO output stage current model shown in Figure 20.
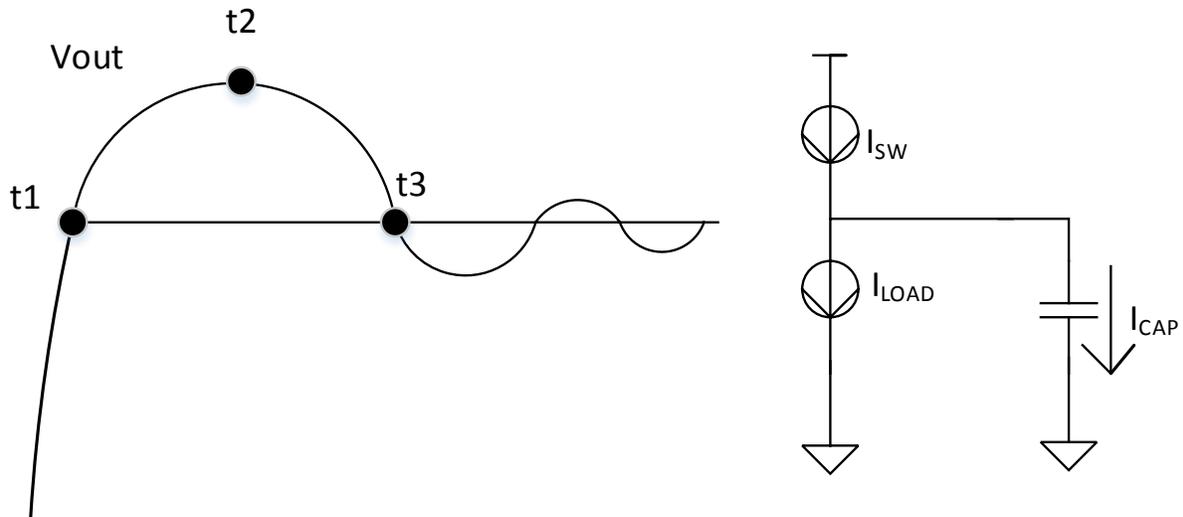
Figure 20 Current at Output Stage for Purposes of Modeling

In the figure, the current through the output of the PMOS is I_{SW}. As can be seen, I_{SW} is equivalent to $I_{CAP}+I_{LOAD}$. I_{CAP} is dependent linearly on the slope of the voltage over time plot. At t_2, the time of the peak, I_{SW} and I_{LOAD} are equal, since I_{CAP} is 0 due to $\frac{dv}{dt} = 0$. Thus, the current through the switch and load is equal, which is indicative of that being the correct number of switches for that state. The output can be modeled as a waveform with equation:

$$v = -e^{-\eta t} * \sin(\omega_0 t) \qquad (4)$$

where η is the damping factor and ϖ_0 is the natural frequency of the system. By analyzing the point at where this equation reaches a local minimum or maximum it is then possible to tell where the number of transistors is at the correct number, since that will be the peak or valley. Since these peaks are generally small relative to the overall voltage in a real circuit, the state at the peak should be close to the state after settling. Thus, taking the number of transistors at the peak should give a good approximation of

the settled number of transistors. Taking the derivative and setting the result to zero

allows the calculation of the local maximum or minimum.

$$\frac{dV}{dt} = -\eta e^{-\eta t} \sin \omega_0 + \omega_0 e^{-\eta t} \cos \omega_0 = 0 \tag{5}$$

This leads to:

$$\omega_0 - \eta \tan \omega_0 t = 0 \tag{6}$$

After taking the arctangent and dividing out the remaining terms this point of time is

found to be related to the natural frequency and damping factor as follows.

$$t = \frac{1}{\omega_0} \tan^{-1} \frac{\omega_0}{\eta} \tag{7}$$

Assuming that the time at the first transition is 0 and the time at the second transition is

$\frac{\pi}{\omega_0}$. The t calculated by equation 7 can then be compared to taking the average time as

the location, as the average time is $\frac{\pi}{2*\omega_0}$. As the arctangent of infinity is $\frac{\pi}{2}$, it can be

observed that at high values of ϖ_0 or low values of η the average time and the peak

time are effectively equal. Since ϖ_0 is generally very large for LDO circuits, it is

expected that averaging will find the number of transistors on at the transition peak.

This should give a rough estimate of the correct state as the peaks are small compared

to the total output voltage.

Section 4.2 Improved Digital Implementation Using Thermometer Encoding

Section 4.2.1 Averaging and Control Circuitry

It is noted that the circuit in [6] used multiple techniques to improve its response;

however, it is desired to look solely at the effect of the averaging circuit. As such, a

design is created to incorporate the averaging. Additionally, the circuit matches as close

as possible to the function presented in [3] when no averaging is performed. Thus, the circuit needs to increment one transistor at a time when there is no crossover and load the average when there is a crossover.

For ease of creating the averaging circuit, the control is setup in binary. A counter is implemented as an eight-bit up/down parallel load counter, which is set to undergo a parallel load if the current state and former state of the comparator differ. This allows single transistor incrementing between transitions of comparator output. In order to eliminate erroneous crossover detection the comparator had an SR latch implemented between it and the rest of the circuit to hold the value of the comparator output until it changed. Two 8-bit registers with enable input are used to store the counter values at the current and previous crossover of V_{ref} and load both to an 8-bit adder. The LSB of the adder output is dropped to conduct a divide by two to find the average. This allows the sum to only change when there is a crossover of the reference voltage rather than at every clock cycle, reducing power consumption. The parallel load is taken instead of incrementing the counter whenever the up/down signal changes. The block diagram for this implementation is shown below. The output blocks will be discussed with the binary to thermometer encoding, as they are effectively the encoder themselves.
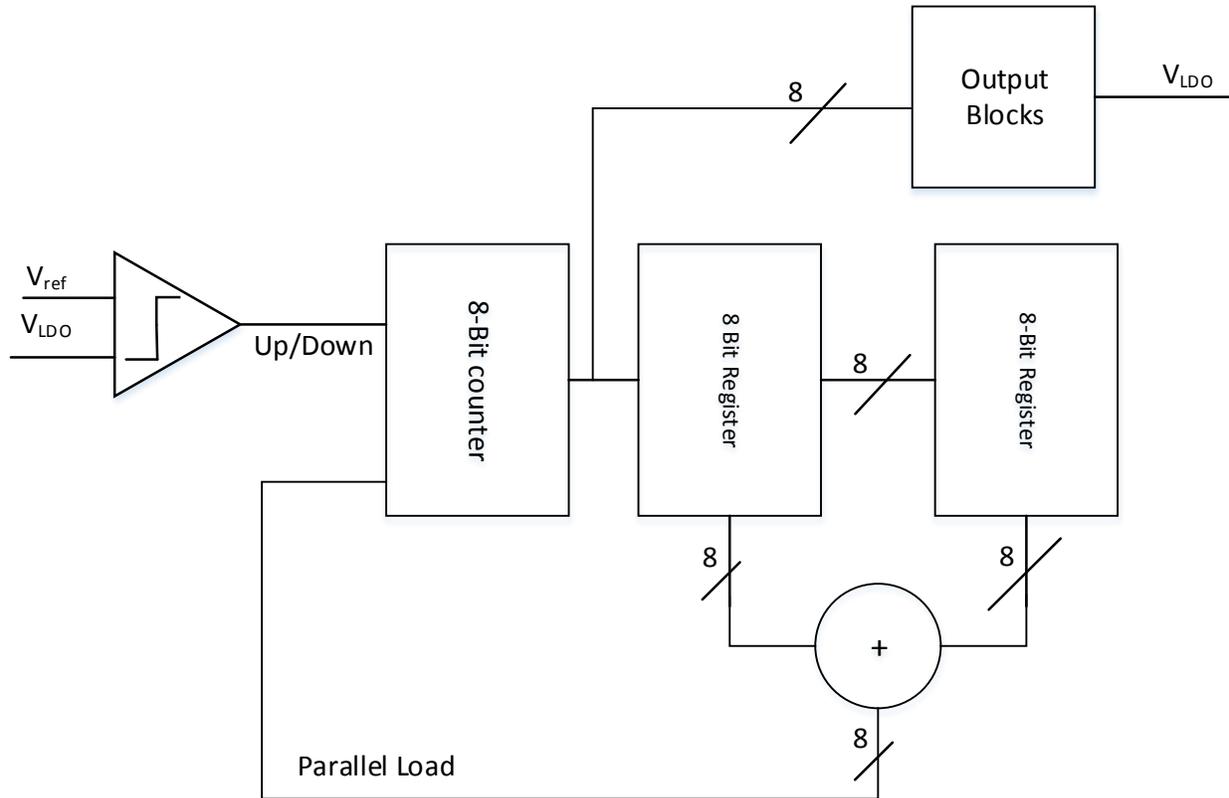
Figure 21 Block Diagram of Circuit Used to Simulate Averaging Effect

Section 4.2.2 Binary to Thermometer Conversion

The averaging circuit can be easily implemented using the binary number system, as shown in Figure 21. However, in the worst-case scenario, 255 transistors are switched at the same time when the circuit goes from 01111111 to 10000000. This creates the problem of both a potential large power consumption due to switching, as well as the possibility of having voltage changes due to switching glitches. To get around this, binary to thermometer code conversion is necessary in order to use thermometer code at the output. The circuit using thermometer code then switches only the number of transistors being switched, similar to the conventional digital LDO.

However, a straightforward 8-bit binary to thermometer conversion circuit is large and difficult to design, as most outputs require knowledge of all eight bits thus leading to complicated logic. A 4-bit binary to thermometer decoder, on the other hand, is simple to implement using two-level logic. A method for using these to convert and control the lines is presented. The goal is to have a 256-bit thermometer code according to the 8-bit counter output.

First, the 8-bit counter output is partitioned into two groups. Each group contains 4 bits. 4-bit binary to thermometer decoder circuits are used to convert them into two groups of thermometer codes. The logic of the 4-bit binary to thermometer code is shown in Table 11. The least significant bit group is passed to the output blocks directly, while the most significant bit group generates an additional thermometer code using XOR gates as shown in Figure 22. All three codes are then passed to the output blocks.

Table 11: 4-bit Binary to Thermometer Logic

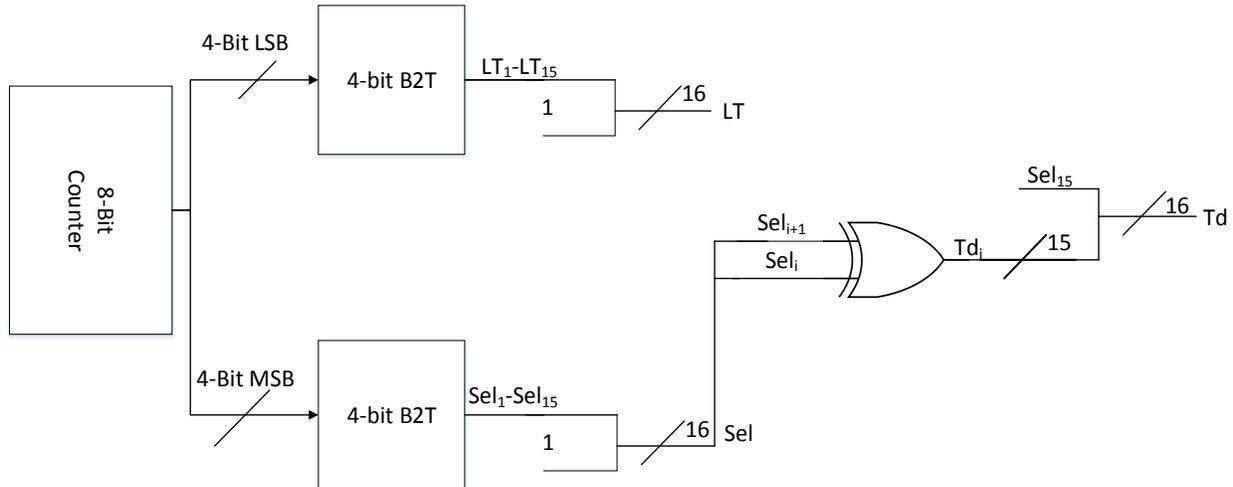| Thermometer Output	Binary Logic
t1	b1+b2+b3+b4
t2	b1+b2+b3
t3	b1+b2+b3*b4
t4	b1+b2
t5	b1+b2*(b3+b4)
t6	b1+b2*b3
t7	b1+b2*b3*b4
t8	b1
t9	b1*(b2+b3+b4)
t10	b1*(b2+b3)
t11	b1*(b2+b3*b4)
t12	b1*b2
t13	b1*b2*(b3+b4)
t14	b1*b2*b3
t15	b1*b2*b3*b4

Figure 22 Control Scheme for 16 Output Blocks of 16 Transistors

It is noted that any binary-to-thermometer encoder will have outputs equal to the

maximum value, so a 4-bit B2T will have 15 outputs, while an 8-bit will have 255. As 15

squared is only 225 that is too few outputs to control 256 transistors, which means that

concatenation is necessary in order to capture 16, rather than 15, signals to pass to the

transistor control from the B2T. The signals that are deemed necessary to pass are the

decoded four least significant bits, a select signal and a last block on signal. These are

labeled as, LT, Sel and Td in the above diagram.

To produce the Td signal for each block, the exclusive-or (XOR) of the chosen

block's select and the next block's select is taken. Save for the final block, as if that

block is on it will use the decoded least significant bit partition as its output regardless of

other information. Hence, the exclusive-or logic gives 15 bits of output with the most

significant bit of the select concatenated on, though in practice this is simply passed to

the blocks continuously. For the select, labeled Sel in the figure, the four most-

significant bits are decoded to 15-bit thermometer code. Since at least one block has to

be active, the circuit simply passes a one to the first block and this becomes the least

significant bit of the block select. Finally, the least significant bits are used to control the

transistors inside the active block. These are decoded and a one is concatenated on as

the least significant bit to make 16 bits.

It should be noted that the above uses a logic 1 to denote the on state. However,

it is necessary to pass 0 to the output transistors for the output transistors to conduct,

since PMOS transistors are used as the power devices. Hence, an inverter is inserted

between the multiplexer and the output. The block diagram is shown in Figure 23.
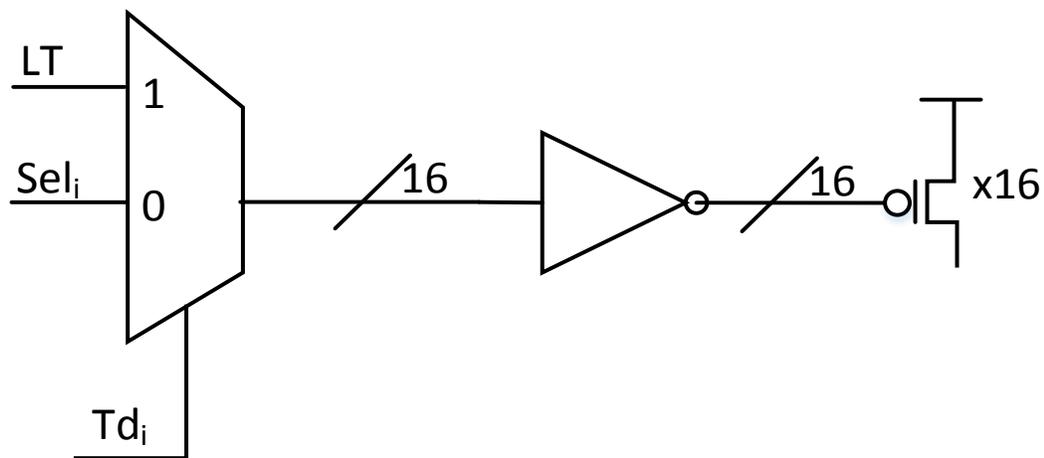

Figure 23 Interior Block Logic

Section 4.3 Simulation Results

Simulations are conducted for the developed circuit with load and line regulation

test settling. The primary factor of interest is the settling time. A 10 Ω ESR is added to

both the reference and the developed circuits. Other parameters are the same as that

used in the previous simulation.
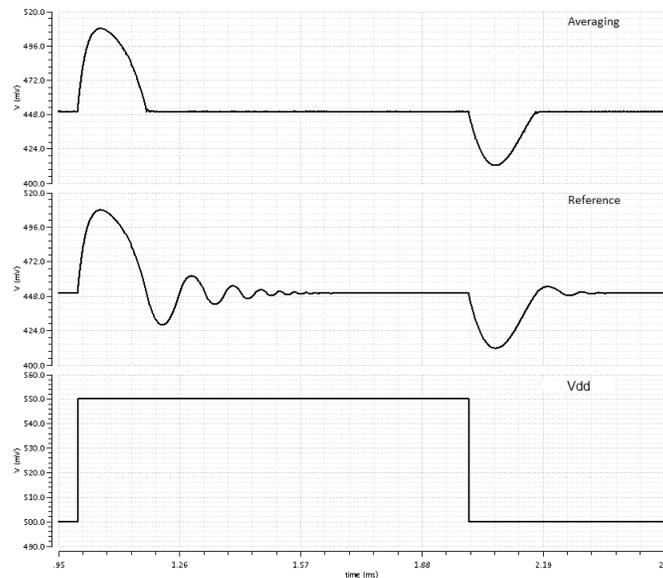
Figure 24 Line Regulation with Averaging Circuit

Table 12: Response to Line Change of Averaging Circuit

Parameter	Reference	Averaging	Improvement
Line Regulation (mV/V)	0.100	0.011	89.2%
Peak on Change (mV)	508.5	508.1	0.8%
Settling on Change (ms)	0.648	0.204	68.6%
Peak on Return (mV)	424.5	424.4	-0.7%
Settling on Return (ms)	0.367	0.202	44.9%

Both voltage changes are analyzed. As summarized in Table 12 and as can be seen from Figure 24, there is no significant difference between the peak of the reference and the developed circuit. However, it shows a large improvement in settling time. The lack of significant difference in peak values validates this test. A significant difference in peak would indicate that the other improvements are affected by the change from shift register to counter based digital control. This also indicates the binary to thermometer coding was successful. The line regulation shows improvement of up to 89% in simulation. However, depending on how exactly the settled voltage is found for

the new design the results exhibit differing amounts of improvement. Thus, it is

uncertain if the advantage is real or a simulation artifact.
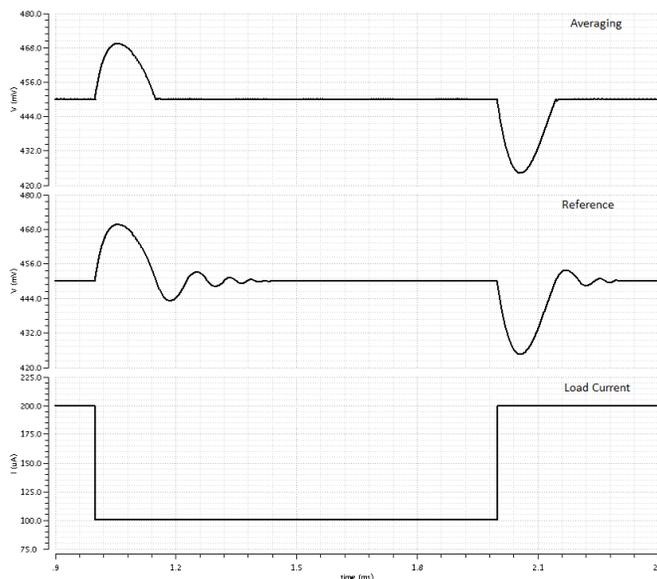
Figure 25 Load Regulation with Averaging Circuit

Table 13: Response to Load Change of Averaging Circuit

Parameter	Reference	Averaging	Improvement
Load Regulation (mV/mA)	0.035	0.019	44.8%
Peak on Change (mV)	469.7	469.4	1.3%
Settling on Change (ms)	0.445	0.176	60.4%
Peak on Return (mV)	411.6	412.4	2.2%
Settling on Return (ms)	0.323	0.167	48.4%

Both current transitions are analyzed. As summarized in Table 13 and as can be

seen from Figure 25, there is no significant difference in the peak from the reference on

either transition with a large improvement in settling time. The load regulation shows

improvement of greater than 60% in simulation. However, depending on how exactly

the settled voltage is found for the new design the results exhibit differing amounts of improvement. Thus, it is uncertain if the advantage is real or a simulation artifact.

With the previous caveats about the regulation, however, it is clear that for both load and line changes the introduction of the averaging circuit drastically improved the settling time with the minimum improvement being an over 44% reduction. This confirms the results in [6], as well as validating the use of the binary to thermometer coding in counter based designs. However, it is noted that the first average after the transition does not give the correct value for number of transistors being on, being up to 30% off. The circuit then immediately has a second crossover of the voltage reference, generating a second average, which is up to 15% off. The justification in section 5.1 indicates these are likely due to the first peak being a significant distance away from the reference voltage. It is considered; therefore, to take the first and second crossovers after the current or voltage switch by means of long transition detection, however, this is found to be slower as the circuit shown settles before the second crossover occurs.

CHAPTER 5

MODELING OF DIGITAL LOW DROPOUT REGULATORS

Section 5.1 Model for PLL Based Designs

This section investigates the modeling of PLL based D-LDO designs as well as the system level effect of applying a multiple-phase comparison technique in place of existing single phased comparison techniques. The multi-phase comparison technique was initially introduced in [7], but its benefits have not been systematically studied yet. The linear circuit model of a PLL based LDO circuit is shown in Figure 26. The VCOs are modeled by the integration block with integration gain of K_{VCO}. The PFDs and charge pump circuit are represented by a phase controlled current source, whose output is given by $\frac{N \cdot \phi}{2\pi} \cdot I_b$. It assumes that each VCO circuit consists of N stages and N PFDs are used for multi-phase comparison. Power transistor M1 is modeled by the voltage control current source with output $g_m \cdot V_g$. Finally, R_2 and C_2 represent the total resistance and capacitance at the output node. The open loop transfer function of the system can be written as:

$$H(s) = \frac{V_{out}(s)}{V_d(s)} = N \cdot A_0 \cdot \frac{\left(1+\frac{s}{\omega_z}\right)}{s^2 \cdot \left(1+\frac{s}{\omega_p}\right)} \tag{8}$$

where $A_0 = \frac{K_{VCO} \cdot I_b}{2\pi \cdot C_1}$, $\omega_z = \frac{\frac{g_m}{C_1}}{1-g_m R_1} \approx -\frac{1}{R_1 C_1}$ if $g_m R_1 \gg 1$, and $\omega_p = -\frac{\left(g_m+\frac{1}{R_2}\right)}{C_2} \approx -\frac{g_m}{C_2}$ if $g_m \gg \frac{1}{R_2}$. When g_m is large and the output node capacitance is small, ω_p is located at high frequency and hence can be ignored. Then, the system has two poles at $\omega = 0$ which introduce an initial 180° phase shift. The zero, ω_z, must be located within the unit gain

bandwidth to make the system stable. This is similar to the stability concern in a type-II phase locked loop (PLL). In such scenarios, increasing the open loop gain will increase the phase margin and enhance system stability. As indicated by Equation 8, the proposed multi-phase comparison technique increases the open loop gain by N, which helps improve the stability of the LDO circuit.

This is also illustrated by the Bode plot of the open loop transfer functions of the LDO circuits with and without the multi-phase comparison technique. The Bode plots shown in Figure 27 are obtained with the following parameter values: $K_{VCO} = 10^9 \, rad/_V$, $I_b = 200 \, nA$, $C_1 = 20 \, pF$, $\omega_Z = 2 \times 10^6 \, rad/_S$, $\omega_P = 10^9 \, rad/_S$, and $N = 3$. Since the proposed technique only increases the DC gain of the transfer function, the two circuits have the same phase responses as shown in the phase plot in Figure 27. In the magnitude plot, the dashed line and solid line depict the magnitude of the transfer functions with and without the multi-phase comparison technique, respectively. In this plot, the proposed technique increases the unit gain frequency from $1.39 \times 10^6 \frac{rad}{s}$ to $3.01 \times 10^6 \frac{rad}{s}$, subsequently improving phase margin from 34.8 to 55.2 degrees. The above analysis assumes that the VCO has three stages. If more stages are used in the VCO design, such as the 13 to 25 stages used in [2], the multi-phase comparison techniques will be more effective on improving the phase margin of the LDO open loop transfer function. Figure 28 shows the phase margin improvement with different N values, starting from an N value of two.
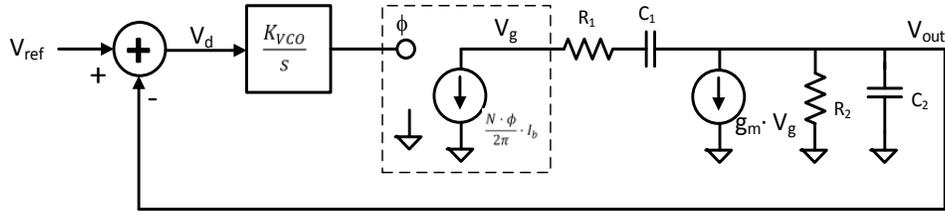
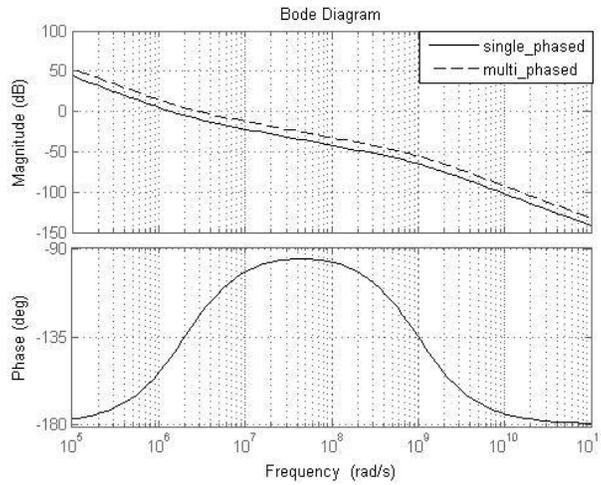*Figure 26 LDO Linearized Circuit Model*

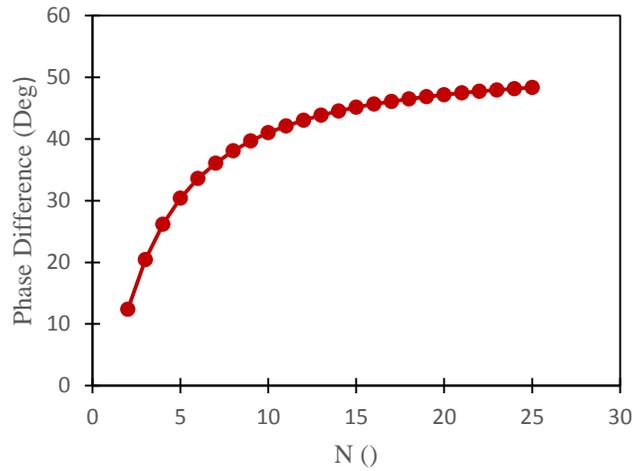*Figure 27 Bode Plot of LDO Circuits with and without Multi-Phase Comparison*

Figure 28 Phase Improvement Efficiency at Different N Values

After ignoring the high frequency pole ω_p, the closed loop transfer function can be simplified as:

$$T(s) = \frac{V_{out}(s)}{V_{ref}} = \frac{N \cdot A_0 \cdot \frac{\left(1+\frac{s}{\omega_z}\right)}{s^2}}{1+N \cdot A_0 \cdot \frac{\left(1+\frac{s}{\omega_z}\right)}{s^2}} = \frac{\frac{2\zeta s}{\omega_n}+1}{\frac{s^2}{\omega_n^2}+\frac{2\zeta s}{\omega_n}+1} \qquad (9)$$

where $\omega_n = \sqrt{N \cdot A_0}$ and $\zeta = \frac{\sqrt{N \cdot A_0}}{2\omega_z}$. Note that the previous LDO design has $\omega_n = \sqrt{A_0}$ and

$\zeta = \frac{\sqrt{A_0}}{2\omega_z}$. The multi-phase comparison technique increases these values by $\sqrt{N}$ times. As

mentioned earlier, A_0 values tend to be small when the power supply voltage is low. This

often results in $\zeta < 0.707$ in realized circuit implementations and hence causes excessive

ripples after load current changes. The proposed technique increases the ζ by $\sqrt{N}$ times

and helps reduce such ripples. In addition, from Equation 10 the loop 3dB bandwidth can

be expressed as:

$$\omega_{3dB} = \omega_n \cdot \sqrt{1 + 2\zeta^2 + \sqrt{(2\zeta^2+1)^2+1}} \qquad (10)$$

Since the multi-phased technique increases both ω_n and ζ by $\sqrt{N}$ times, it increases ω_{3dB}

by at least $\sqrt{N}$ times. This increased loop bandwidth helps improve the circuit transient

response. With the aforementioned parameter values, the step responses of the LDOs

with and without the multi-phase comparison technique are compared in Figure 29. It

clearly shows that a design with multi-phased comparison exhibits smaller overshoot and
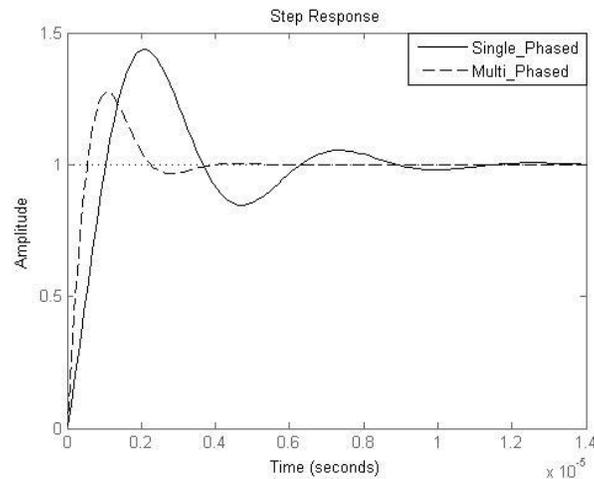
settles faster.

Figure 29 Step Responses of LDO Circuits with and without Multi-Phase Comparison

Section 5.2 Simulink Model of Digital LDO

Both the z-domain and s-domain transfer functions of digital LDOs reported in literature are open loop transfer functions. It is difficult to use them to estimate closed loop behavior due to the nonlinearity of the comparator gain. To address this problem, a Simulink model is developed in this section for estimating the LDO behavior with different design parameters. The proposed Simulink model is shown in Figure 30. Since this is similar to AC analysis, the reference voltage is a constant in the circuit and subsequently treated as 0 in the model.
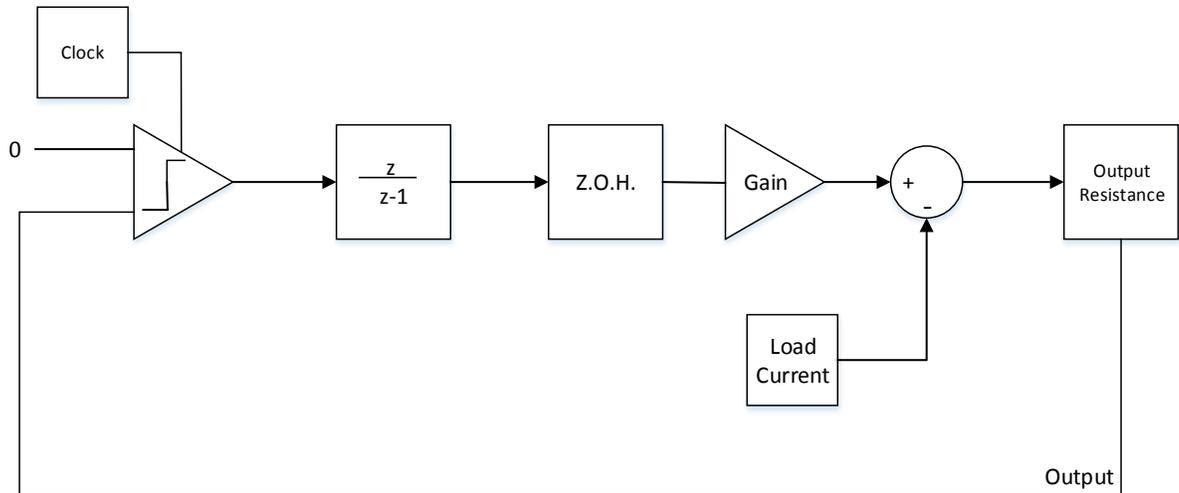
Figure 30 Block Diagram of Simulink Model

The parameters for each block that is included in this model will be discussed along with what they represent. Starting from the comparator, the comparator block is implemented using a relationship operator set to compare the output with 0. A latch block is used to make the system discrete time. A clock set at the desired frequency controls the comparator. The next block is a z-transfer function block to model the integrator; this is simply $\frac{z}{z-1}$ and will not change regardless of the rest of the circuit, as the integrator is common across the investigated LDO circuits. It is followed by a zero order hold, which models the holding of the state by the shift register or counter. Both of these have their sample times set to the clock frequency for proper operation.   A gain block is then used to convert the number of transistors to a current and correct, if necessary, the comparator block gain. Thus, the gain value is the correct amount of current per power transistor. For example, in the model tested the comparator output is set to -0.5 or 0.5 when it should have been -1 or 1 to indicate turning off or on a transistor. Also, assume the current conducted by a single transistor is I_{PM}. The gain

value should be 2*I$_{PM}$. The gain here depends on the sizing of the output transistors in the circuit under test, so this part of the model requires knowledge about the circuit to be implemented. The next step is to find the net current, as the voltage drop across the transistors is the net resistance seen by the output line times the current conducted by the transistors above or below the load current. Thus, the net current is the amount of current conducted by the transistors, which is given by the gain block output minus the load current. The output of the subtraction is the total output current the output resistance conducts, which gives the output voltage by Ohm's law.

The output resistance is a variable resistor that is modeled as the small signal resistance as seen by the output voltage. This depends on the output current, output capacitor, equivalent series resistor, and voltage drop across the PMOS. For the purposes of this model it is assumed that the capacitive branch of the output conducts little current compared to the load current, thus making the load current equal the output current. The voltage drop models the sum resistance of the PMOS transistors across them divided by the current across them. The small signal model is shown in Figure 31, below.
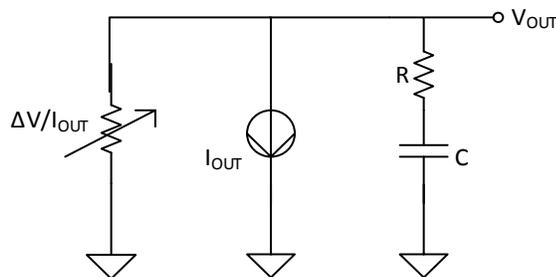

Figure 31 Small Signal Model of Resistance as Seen by Output

This model is then used to calculate the equivalent resistance. Since I_{OUT} is treated as an ideal current source, it has an infinite resistance and drops out. This leaves the equation:

$$R(s) = \frac{\Delta V}{I_{OUT}} \,||\, \left(\frac{1}{sC} + R\right) \,||\, \infty = \frac{\frac{\Delta V}{I_{OUT}} * \left(\frac{1}{sC} + R\right)}{\frac{1}{sC} + R + \frac{\Delta V}{I_{OUT}}} \tag{11}$$

If the equation is simplified it takes on the appearance of a one pole, one zero transfer function multiplied by a resistance, as shown in Equation 12.

$$R(s) = \frac{\frac{\Delta V}{I_{OUT}} * (1 + sRC)}{1 + s\left(R + \frac{\Delta V}{I_{OUT}}\right)C} \tag{12}$$

As such, an s-domain transfer function block is utilized to hold the resistance equation and convert the current back to the output voltage. The equivalent series resistance (ESR) is likely to be much smaller than the equivalent resistance of the transistors. Thus, it is likely that in most cases the ESR will add a zero without significantly affecting the pole frequency. As this model looks at current changes, it is necessary to know whether to use the low or high current for this model. The low current parameters are found to dominate on transitions, and so are used as the I_{OUT} parameter.

This model is tested with 1, 10 and 20 MHz clocks and load current transitions of 100 to 150 µA, and 200 to 100 µA. The obtained results are compared with LDO circuit simulation data. The output parameters chosen are a 10-Ω output series resistor with 100 nF capacitor. As such, the resistance mentioned above was set constantly as shown in Equation 13.

$$R(s) = \frac{\frac{50\ mV}{100\ \mu A}(1 + s * 10\Omega * 100nF)}{1 + s\left(\frac{50\ mV}{100\ \mu A} + 10\right)100nF} = \frac{500 * 10^{-6} * s + 500}{51 * 10^{-6} * s + 1}\Omega \qquad (13)$$

These resulted in the plots in Figure 32. In each plot, the dashed line is the data from

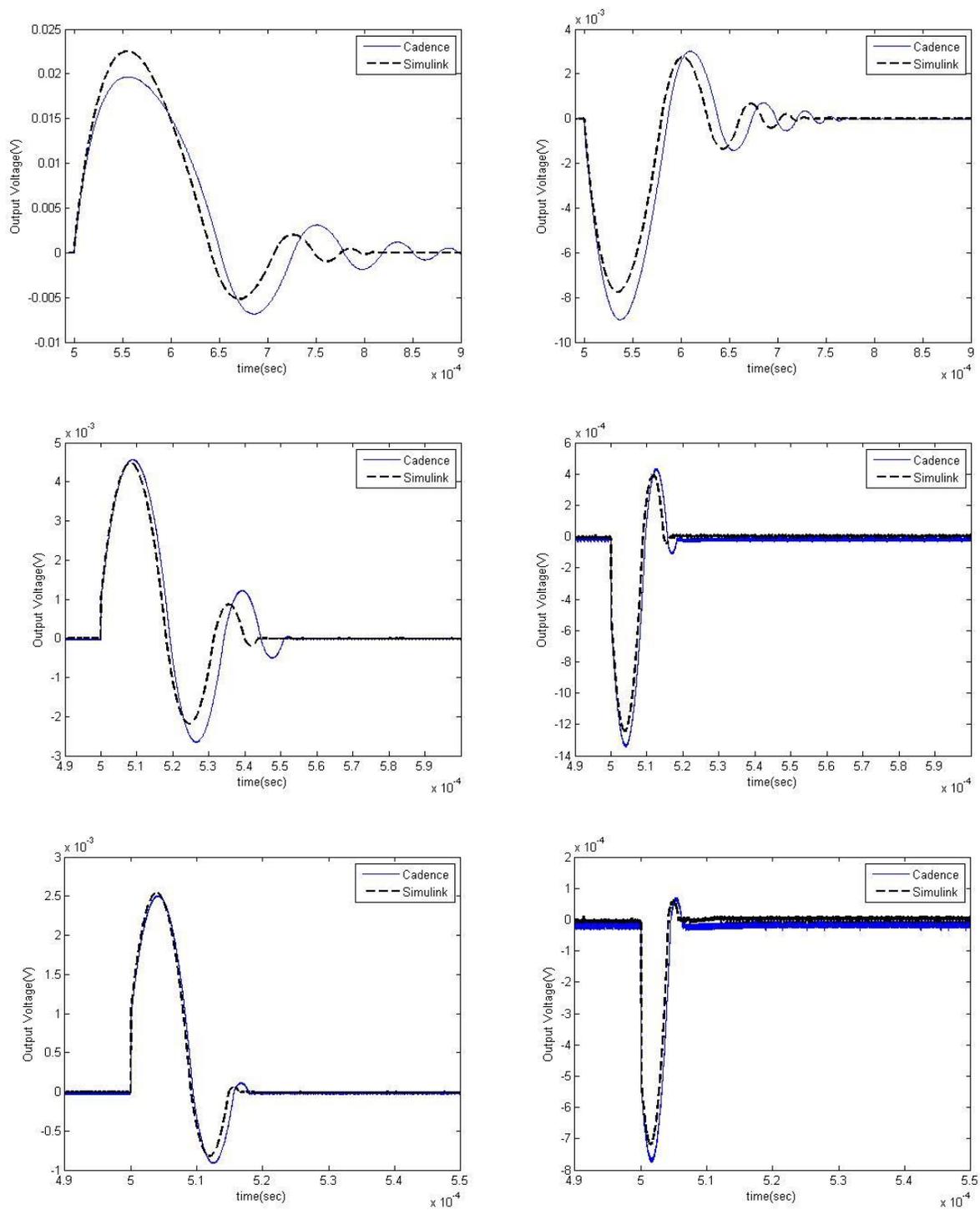the Simulink model, and the solid line is the circuit simulation result.

Figure 32 Simulink and Cadence Simulation Comparison; Top 1 MHz Clock, Middle 10 MHz Clock, Bottom 20 MHz Clock; Left High to Low Transition, Right Low to High Transition

It can be seen that the simulations at the circuit level and at the system level in Simulink give close results for the settling time and peaking. The results for peak and settling are shown below. The peaks have a maximum error of less than 20%, while the settling error was below 20% on all except for the high to low transition at the slowest clock. The results are split out by transition for ease of reading.

Table 14: Simulation Comparison on High to Low Current Transition

Clock Frequency	Peak (mV)	Settling Time (µs)	Peak (mV)	Settling Time (µs)	Peak Error	Settling Error
Simulation	Cadence	Cadence	Simulink	Simulink	N/A	N/A
1MHz	18.9	680	22.5	319	19.0%	53.2%
10MHz	5.087	53.6	4.484	46.8	11.9%	12.7%
20MHz	2.527	18	2.545	16	0.7%	8.4%

Table 15: Simulation Comparison on Low to High Current Transition

Clock Frequency	Valley (mV)	Settling Time (µs)	Valley (mV)	Settling Time (µs)	Valley Error	Settling Error
Simulation	Cadence	Cadence	Simulink	Simulink	N/A	N/A
1MHz	9	290	7.709	240	14.3%	17.2%
10MHz	1.331	16.3	1.244	18.3	6.5%	12.3%
20MHz	0.7631	6.8	0.712	7.5	6.7%	10.3%

CHAPTER 6

CONCLUSIONS

Several techniques for modeling and improvement of digital LDO transient response are discussed in this thesis. It is also found that the ESR of the output capacitor has dramatic impact on LDO settling behavior. A Simulink model is proposed for estimating the response to current changes of a digital LDO. This thesis also investigates the effect of multi-phase comparison on a PLL based digital LDO, which increases the loop gain and significantly improves LDO transient response. In addition, two modifications to digital LDO circuits are examined. The attempt to add a capacitive feedback loop to the output of a digital LDO is concluded to be too vulnerable to glitches to be practical, though it significantly reduces the ripple when the ripple is large enough to mask the effects of the glitch. A method of using a numerical method to reduce settling time by using an averaging method is also investigated. It significantly reduces the settling time, as well as improves regulation.

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