Spring 1-28-2018

A 5.8 GHz DSRC Digitally Controlled CMOS RF-SoC Transceiver for China ETC

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Abstract – This paper presents a 5.8 GHz dedicated short range communication (DSRC) CMOS RF-SoC transceiver with digitally controlled RF architecture for China electronic toll collection (ETC) system. The operation of key RF blocks, such as ASK modulator, power amplifier, LNA, and mixer, are directly controlled by digital baseband. Compared with state-of-the-art designs in literature, this work demonstrates remarkable advantages in design simplicity, Tx output peak power, adjacent channel power ratio (ACPR), dynamic range, occupied bandwidth (OBW), bit error rate (BER), and so on.

I. Introduction

ETC systems have been widely used as a smart transportation solution, where dedicated short-range communication connects a toll system with end users via 5.8 GHz wireless communication. As a critical component, a transceiver for ETC systems demands low design complexity, high receiver sensitivity, low bit error rate (BER), occupied bandwidth (OBW) and adjacent channel power ratio (ACPR), wide dynamic range, small system size, low cost, etc. In literature, all existing transceiver architectures are based on analog control approach, which inherently requires large circuit area, high design complexity, and weak reconfiguration. Therefore, it is necessary to investigate new transceiver architectures to meet all these system requirements.

This paper presents an efficient design of 5.8 GHz DSRC digitally controlled CMOS transceiver for China ETC systems. All building blocks (*i.e.*, LNA, mixer, power amplifier, ASK modulator) are digitally controlled by baseband, thus eliminating non-essential analog blocks (*e.g.*, filter, DAC, voltage-current converter). Besides, digital control leads to great system flexibility and a wider dynamic range. In addition, digital control is adaptive to technology scaling. It is easy to migrate and implement in different CMOS process. To the best of our knowledge, this is the first work to integrate all RF, IF blocks and digital baseband to realize an RF-SoC solution.

II. Proposed Transceiver Architecture

Fig. 1 illustrates the proposed architecture of digitally controlled transceiver, which consists of a wake-up block (WuRx), a receiver (Rx), a transmitter (Tx), a PLL, a power management block, and a digital baseband. In the transmitter block, the input digital signal (D_{TX}) directly modulates 5.8 GHz RF carrier from PLL. The control signals from digital baseband dynamically adjust the gains of ASK modulator and PA blocks. Fig. 2 and 3 show the circuit schematics of proposed digitally controlled ASK modulator and PA. In Fig. 2, a 5-bit control word (*BB_Data<4:0>*) involves 32 tuning steps for ASK modulation adjustment. Discrete levels of modulation index are achieved without using expensive analog blocks (e.g., PSF or DAC converter) [2]-[3]. This ASK modulator avoids LO leakage issue to RF output as the case using mixers, since the LO signal is directly modulated by digital control. The PA in Fig. 3 has four gain levels, which are determined by the digital signal (*C<2:0>*). The output power of PA linearly varies with these four gain levels. In the receiver side, the received signal (RX_{IN}) from antenna changes as a vehicle passing through. To ensure continuous coverage for various input power levels, automatic gain control (AGC) is desired to intelligently adjust the gains of LNA, mixer, and PGAs. Thus, the IF signal into the main ADC fits well with its input range. Similar to Fig. 2 and 3, the schematics of LNA, mixer, and PGAs in our architecture are designed for digital control. Digital AGC is implemented in baseband and achieves higher accuracy via sophisticated algorithms. It is flexible and convenient for designers to revise the AGC algorithm without re-designing any sensitive RF/analog blocks.

III. Experimental Results

This 5.8 GHz DSRC transceiver chip for China ETC system was fabricated in a 0.13μm CMOS process. Fig. 4 shows the die micrograph and chip measurement environment. Due to it is a fully integrated RF-SoC, off-chip passive components are minimized from chip test board. Table 1 summarizes and compares this work with reported state-of-the-art works in the literature.

In the transmitter mode, Fig. 5 presents the measured waveform of ACPR, which is limited below -38dBc @ 5MHz offset. Fig. 6 presents the measured result of OBW. Fig. 7 plots how the transmitter output power varies with modulator step and power gain level. A fine-grained transmitter output power is observed using the combination of digitally controlled modulator step and PA gain level. The maximum output power of a single-ended port is 7.23 dBm, considering an approximate test cable loss of 3dBm. The transmitter dynamic range is wider than [1] and [3]. In the receiver mode, the measured receiver sensitivity is -75dBm. Measurement results show the best BER and the widest dynamic range. When the BER is below 10-6, the receiver dynamic range of this design is -75dBm ~ -8dBm, which indicates an increase of 89% than [1] and 12% than [3]. Overall, the proposed design achieves the minimum system size, which is 34% smaller than [3].

IV. Conclusion

This paper presented a design and implementation of 5.8 GHz CMOS DSRC transceiver for China ETC. Digital control is used to adjust the operation of RF blocks. To our best knowledge, this is the first RF-SoC integration for ETC application. Compared with prior designs, various chip measurement results demonstrate significant performance enhancement, low-cost implementation, and less design complexity.

References

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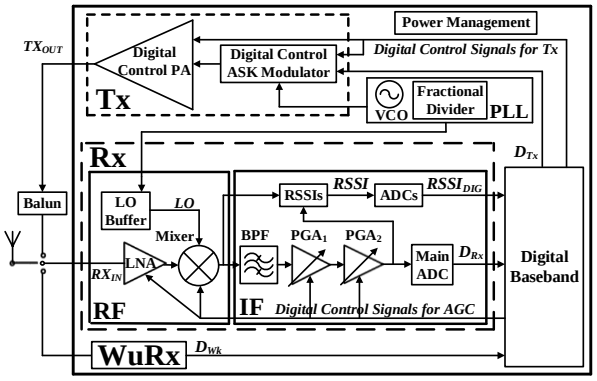

Fig. 1. Block diagram of the proposed digitally controlled DSRC transceiver architecture in China ETC system

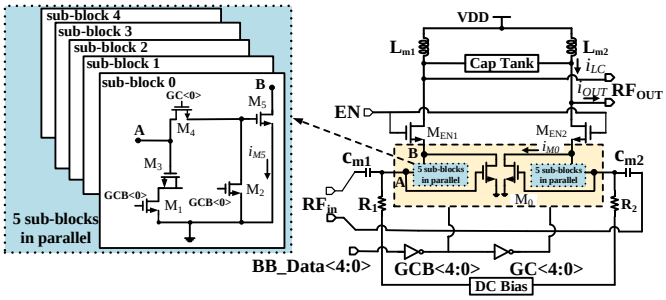

Fig. 2. Circuit schematic of the proposed digitally controlled programmable ASK modulator

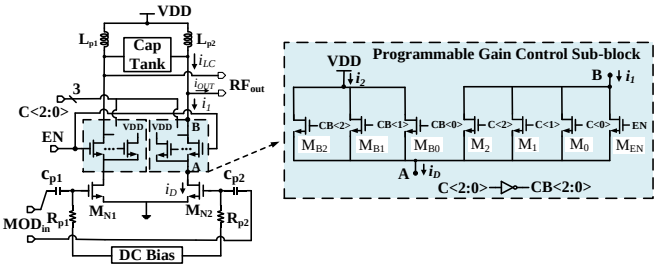

Fig. 3. Circuit schematic of the proposed digitally controlled programmable gain power amplifier

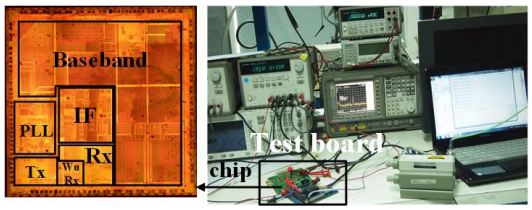

Fig. 4. Die microphotograph and chip measurement environment

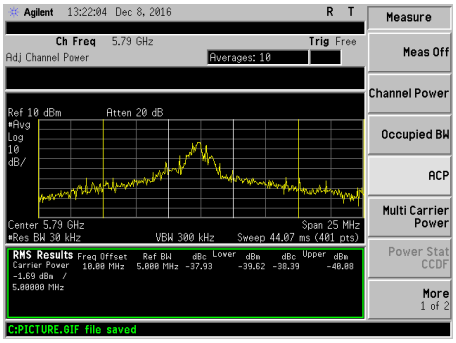

Fig. 5. Measurement results of ACPR

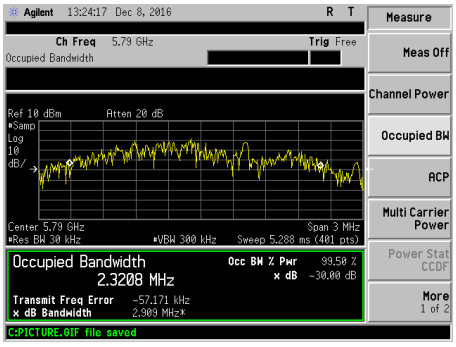

Fig. 6. Measurement results of OBW

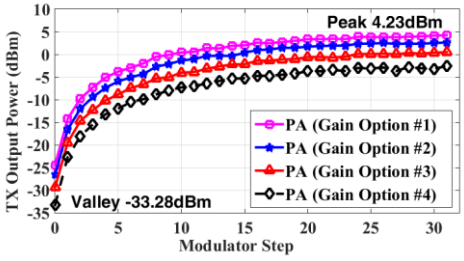

Fig. 7. Measurement of transmitter output power

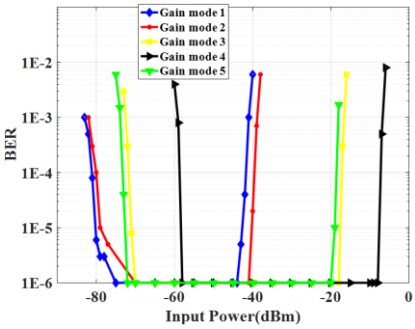

Fig. 8. Measured BER with five gain mode settings

Table 1. Comparisons of this work with state-of-the-art 5.8 GHz DSRC transceiver chips

Reference	Tx output peak power (dBm)	OBW (MHz)	ACPR (dBc)	Tx dynamic range (dB)	Rx dynamic range (dBm)	BER	AGC	Area of RF blocks (mm^2)	Current consumption of RF blocks (mA)
[1]	+10.5 (differential)	2~6	-49 (+6MHz)	19	-76 ~ -40	N/A	Limited	N/A	51
[2]	+10 (differential)	N/A	-43 (+10MHz)	N/A	-84 ~ N/A	10^{-5}	Limited	3.31	N/A
[3]	+5 (single end)	3	-53 (+10MHz)	34	-60 ~ 0	N/A	No	2	59
This work	+ 7.23 (single end)	2	-38 (+5MHz)	37	-76 ~ -8	10^{-6}	Yes, on-chip	1.32	58