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A Fully Integrated RSSI and an Ultra-Low Power SAR ADC for 5.8GHz DSRC ETC Transceiver

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***Abstract*: This study presents a monolithic received signal strength indicator (RSSI) and an ultra-low power SAR ADC for 5.8GHz DSRC transceiver in China electronic toll collection systems. In order to meet the stringent requirement of wide input range for the transceiver, two RSSIs collaborate with auxiliary ADC circuits to provide the digitalized received signal strength to the digital baseband of a transceiver. The RSSI design achieves fast transient response, low power consumption, and a small die area with internal active low-pass filters instead of external passive ones. The proposed design has been fabricated using a 0.13μm 2P6M CMOS technology. Measurement results show that the overall input dynamic range is 86dB with an accuracy of ±1.72dB and a transient response of less than 2μs. Compared with the state-of-the-art designs in the literature, the overall input range and transient settling time are improved by at least 14.6%, and 300%, respectively.**

Keywords—RSSI, ADC, electronic toll collection, fully integrated, ultra-low power

I. Introduction

Electronic toll collection (ETC) systems are widely deployed in intelligent transportation systems around the world. In 2015, Chinese Ministry of Communications issued the latest Chinese ETC standard, which adopts Amplitude Shift Keying (ASK) modulation and Dedicated Short Range Communication (DSRC) at 5.8 GHz. A complete ETC system consists of road side units (RSU) and an on-board unit (OBU). An OBU system requires low cost, small form factor, low power, good reliability, large dynamic range, and long battery life [1-2]. An on-chip fully integrated design, which is composed of RF, analog, and digital baseband circuits, is well suited to meet these requirements in OBU systems.

The amplitude of input signal received at an OBU typically varies significantly. A received signal strength indicator (RSSI) circuit can be used to detect and inform the input signal level to the baseband of an OBU system, which runs an automatic gain control (AGC) algorithm to adjust the receiver gain and ensure continuous coverage (*i.e.*, no dead zone) for a wide range of input power levels (*e.g.*, 80dBm). AGC demands a wide dynamic range, good linearity, and fast settling time of RSSI circuits [3]. Moreover, since the OBU system is battery powered and attached to a vehicle window, it is desired to minimize power

consumption and limit off-chip components to improve user convenience and system size. However, up to date, traditional RSSI circuits [3-7] [10] and [12] have difficulties to realize wide input ranges (*e.g.*, 80dBm). These RSSIs also exhibit slow transient response, high power consumption, and low level of system integration due to the use of large off-chip capacitors. Therefore, it is attractive to develop novel RSSI circuits or system architectures that enable higher levels of system integration, a wider input range, lower power consumption, and faster settling time. This is the focus of this paper.

This work makes the following contributions: (a) a new DSRC transceiver architecture is proposed, where two identical RSSI circuits work together to achieve a wide dynamic range. Each RSSI circuit consists of only on-chip devices, resulting in a much smaller die size while achieving fast settling time and low power consumption. To the best of our knowledge, this is the first work in the literature to present design details of monolithic RSSI circuits. (b) We have implemented and fabricated the proposed RSSI design with an ultra-low power SAR ADC in a standard 0.13μm CMOS technology. Measurement results demonstrate the benefits of this proposed design in terms of chip area, detection accuracy, power consumption, input dynamic range, and transient response. Compared with the state-of-the-art designs in the literature, the overall input dynamic range and transient settling time are improved by at least 14.6%, and 300%, respectively.

This rest of this paper is organized as follows. In Section II, the proposed RSSI architecture in a 5.8GHz DSRC transceiver is presented and analyzed. The details of RSSI circuit analysis and implementation are described in Section III. Chip measurement results are introduced and discussed in Section IV. Section V concludes the paper.

II. Proposed RSSI Architecture

A. DSRC Transceiver Architecture

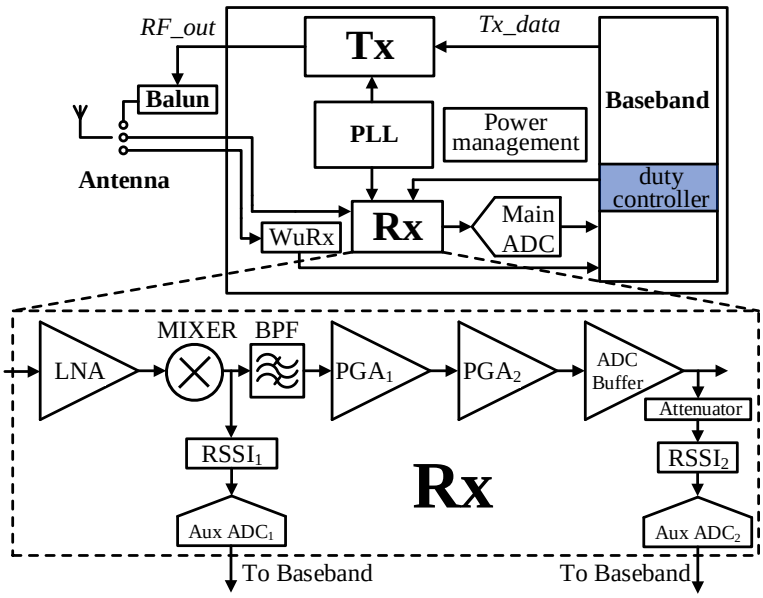


Fig. 1. Overall architecture of the developed 5.8 GHz DSRC RF-SoC transceiver

Fig. 1 illustrates the overall hardware architecture of a 5.8GHz DSRC transceiver, which includes a wake-up block (WuRx), a receiver (Rx), a transmitter (Tx), a phase-locked loop (PLL), a power management block, and a baseband. The entire system operates in three

modes: Tx, Rx, and sleep. The signal from/to antenna is controlled by baseband to switch among Tx, Rx, and WuRx blocks. A wake-up receiver (WuRx) is required to achieve long battery life. The WuRx block is only active in standby mode. The PLL, which includes LC-VCO block, offers local oscillator (LO) signal for Rx and Tx. To reduce power consumption, a duty controller is also realized in the baseband to enable/disable the Rx.

Rx is composed of a low-noise amplifier (LNA), a down-conversion mixer (MIXER), a band-pass filter (BPF), RSSI circuits ($RSSI_1$ and $RSSI_2$), programmable gain amplifiers (PGA_1 and PGA_2), auxiliary ADCs (Aux ADC_1 and Aux ADC_2), a main ADC buffer, and an attenuator for AuxADC_2. The BPF is inserted between the MIXER and PGA_1. Thus the out-of-band noise and spur, such as flicker noise and DC offset at low frequency, adjacent-channel signals at high frequency, can be removed before the in-band signal is passed into PGA_1. The in-band noise can be avoided by using an active BPF with a 10dB gain. The received signal strength has a large variation when a vehicle approaches an ETC system. In order to keep an appropriate signal level into the main ADC in Fig. 1, it is necessary to adjust the gain of each block in the Rx according to the detected signal strength. In the proposed architecture, two RSSI blocks ($RSSI_1$ and $RSSI_2$) and two auxiliary ADC blocks are embedded in Rx. The received input signal strength from the antenna is assessed by two RSSIs and then digitized by the subsequent auxiliary ADCs. The digitized RSSI signals are provided to the baseband. Our system relies on an AGC algorithm to control the gain of each block in Rx.

Fig. 2 depicts the flowchart of proposed AGC algorithm. Once the Rx is enabled, gains of Rx circuits enter to gain mode 1. Then, the $RSSI_1$ circuit begins to detect the signal power. After the digitized $RSSI_1$ signal is provided to the baseband, based on the signal range of $RSSI_1$, the gains of LNA, MIXER, and PGA_1 will be adjusted. For example, if the received input signal is within the range 4, gain mode 3 is first applied. Then, the $RSSI_1$ value is assessed again, the gain mode of LNA, MIXER, and PGA_1 is updated accordingly. Finally, $RSSI_2$ begins to detect the signal magnitude. Based on the value of $RSSI_2$, the AGC algorithm will regulate the gains of PGA_2 and ADC buffer. Both RSSIs are always detecting the signal strength, the baseband decides which one to read at any given time.

Fig. 3 plots the gain settings of $RSSI_1$ and $RSSI_2$ circuits for different input signal strength according to the proposed AGC algorithm. LNA has three gain options: maximum (Max), middle (Mid), and minimum (Min). MIXER and PGA_1 have two gain options: maximum (Max) and minimum (Min). As the gains of BPF and attenuator circuits are fixed, both circuits are not varying with the signals of $RSSI_1$ and $RSSI_2$. The gains of LNA, MIXER, and PGA_1 are adjusted according to the $RSSI_1$ reading. The gains of PGA_2 and ADC buffer are adjusted after reading the $RSSI_2$ value. In this design, LNA, MIXER, and PGA_1 support coarse gain adjustment, while PGA_2 and ADC buffer support fine gain adjustment. After reading $RSSI_1$, the gain modes of LNA, MIXER and PGA_1 are determined as listed in Table I. After reading $RSSI_2$, the gain modes of PGA_2 and ADC buffer are finalized by the complete AGC algorithm in digital baseband. If there is no convergence when reading $RSSI_2$, the AGC algorithm will return to start over. According to entire system requirements, the targeted input power levels is from -86dBm to 0dBm. As the input signal passes through the LNA, MIXER, PGA_1 and PGA_2 in Fig. 1, each RSSI only needs to handle a portion of the whole input signal range. For design simplicity, two RSSIs are designed to be identical, and used at different locations of signal path where signal strength to be detected is distinct. An attenuator added to $RSSI_2$ to accommodate the higher power level and ensure proper detection range for $RSSI_2$. Observed from Fig. 3, an operation range of 40dB is sufficient for each RSSI circuit.

TABLE I. Summary of gain settings of various blocks in targeted receiver input power range

Gain mode	Receiver input power (dBm)	LNA gain (dB)	MIXER gain (dB)	PGA_1 gain (dB)	PGA_2 gain (dB)	ADC buffer gain (dB)
1	-86 ~ -65	Max	Max	Max	Setup by complete AGC algorithm in digital baseband for fine gain control	
2	-65 ~-53	Max	Max	Min		
3	-53 ~ -38.5	Mid	Min	Max		
4	-38.5 ~ 28	Mid	Min	Min		
5	-28 ~ 0	Min	Min	Min		

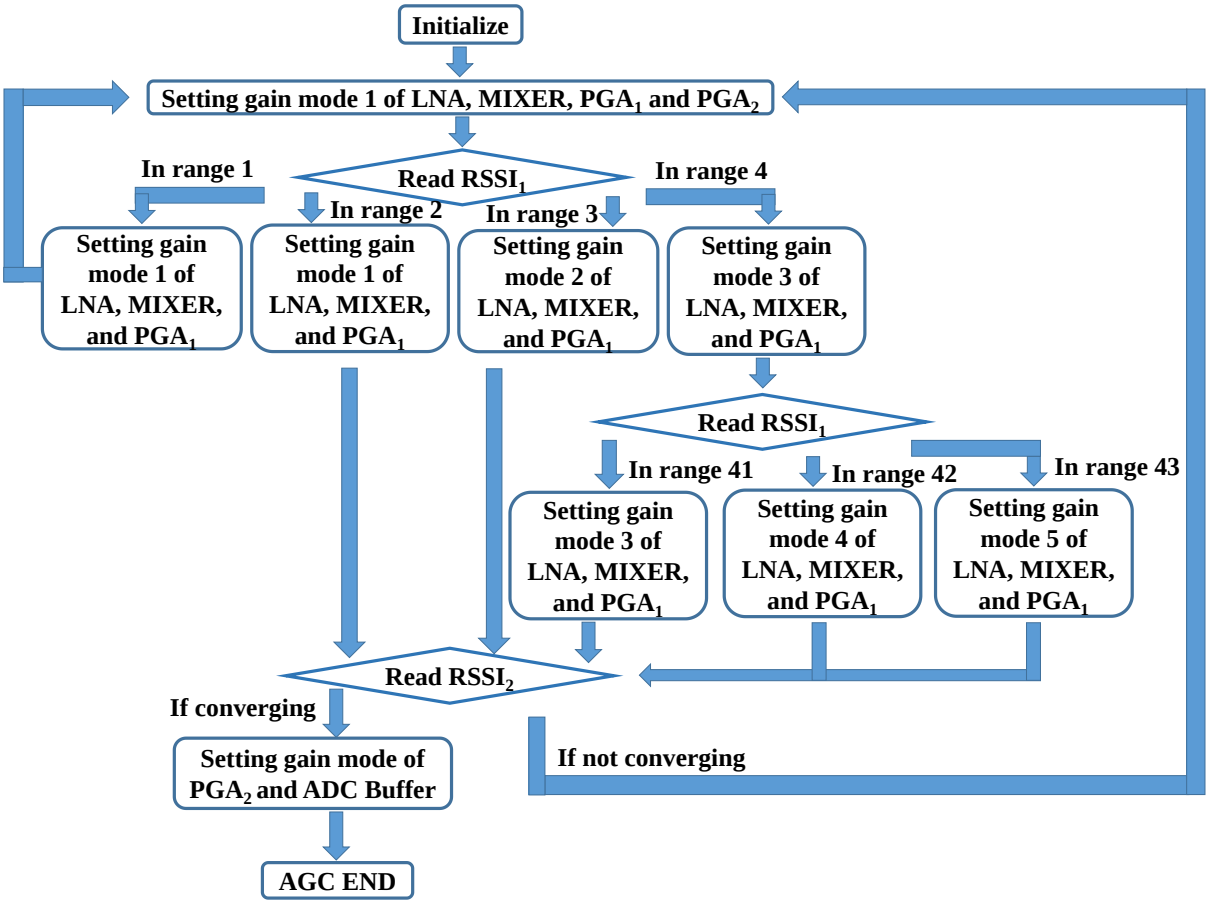


Fig. 2. AGC flow and RSSIs setting flow

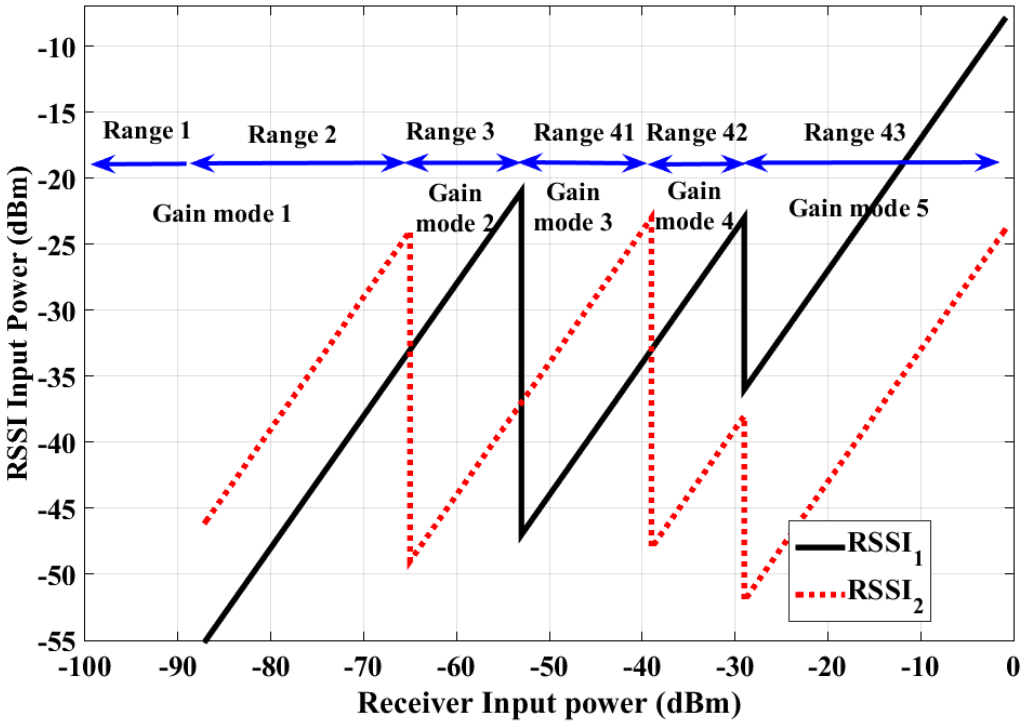


Fig. 3. Proposed range settings and gain modes of our RSSI circuit

B. Conventional RSSI Architecture

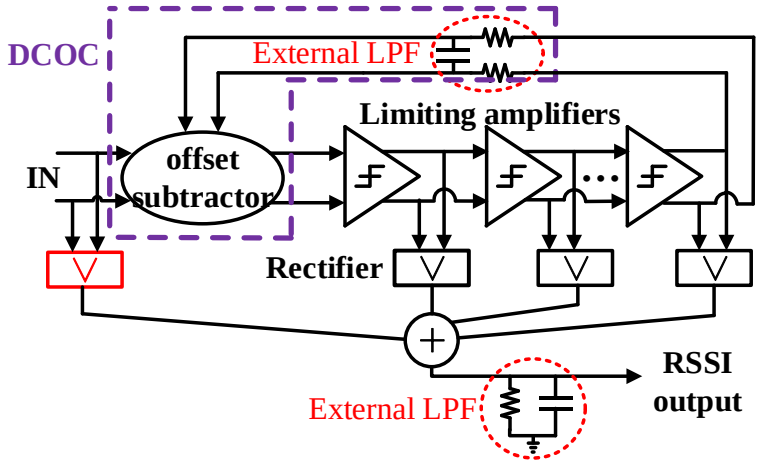


Fig. 4. Conventional RSSI circuit architecture

Fig. 4 depicts the conventional RSSI architecture, which consists of a dc offset subtractor, a summer circuit, two external passive low-pass filters (LPFs), several limiting amplifiers and rectifiers for successive detection [5, 8-9]. The traditional RSSI circuit is based on passive low-pass filters with discrete RC components. In order to achieve low bandwidth, large capacitance and resistance are required in passive low-pass filters. Due to big area overhead, capacitance usually does not integrate on chip. Therefore, extra pads and wiring metal are used for off-chip capacitor connection. In contrast, fully integrated active LPFs have the advantages of being smaller, lighter, more reliable and less expensive. The dc offset cancellation (DCOC) loop includes external LPFs, which increases chip area. The input signal is processed through this amplifier chain. In each stage, the voltage signal is converted into current domain with a logarithmic transfer function. The summer circuit superimposes

output currents of all stages. Then, another external LPF filters out AC components and converts the total current into a voltage as the RSSI output. The use of two external passive LPFs excludes monolithic integration, increases chip area and signal settling time.

C. Proposed RSSI architecture

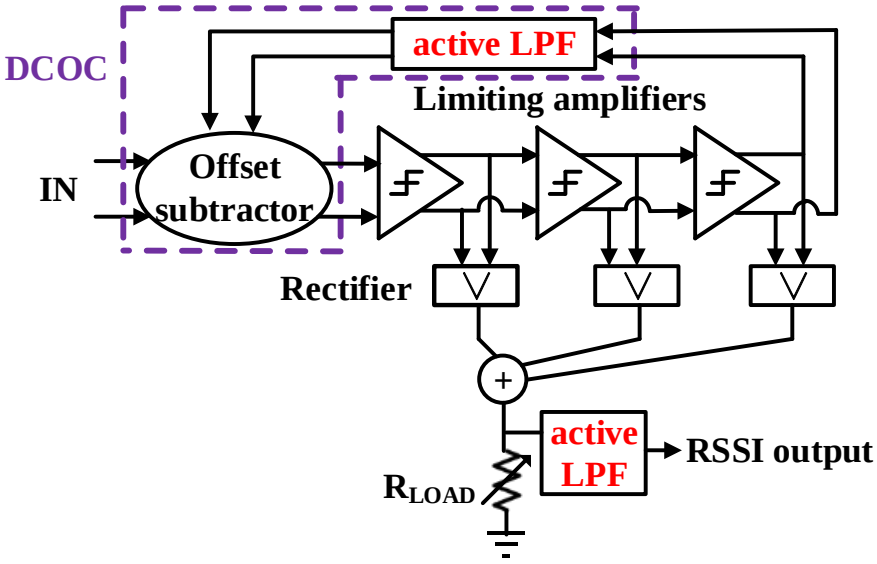


Fig. 5. Proposed RSSI circuit architecture

A new RSSI architecture is proposed in Fig. 5, where the most left rectifier is removed and two external LPFs are replaced. The input signal is amplified by three cascade limiting amplifiers. Three rectifiers convert the output signals of these limiting amplifiers into a current. If the input signal is very small, the RSSI output voltage is also small. Thus, it leads to a bad signal to noise ratio (SNR) of subsequent auxiliary ADC and hence degrades the performance of AGC algorithm. To address this challenge, a novel summer circuit is proposed, which superimposes the output currents of rectifiers and the bias currents. Note the bias currents do not vary with the RSSI input, so the bias currents can be treated as constants. To mitigate the impact of process variation, two calibration schemes are developed to change bias currents and adjust the load resistor (R_{LOAD}) through digital baseband.

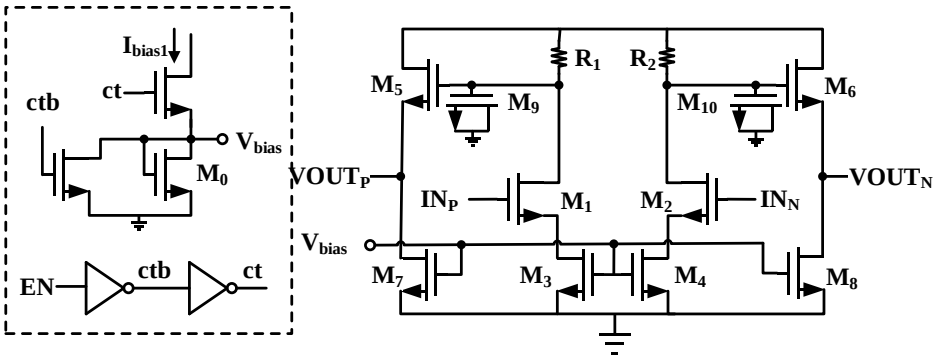
III. RSSI Circuit Implementation

A. Limiting amplifier and rectifier

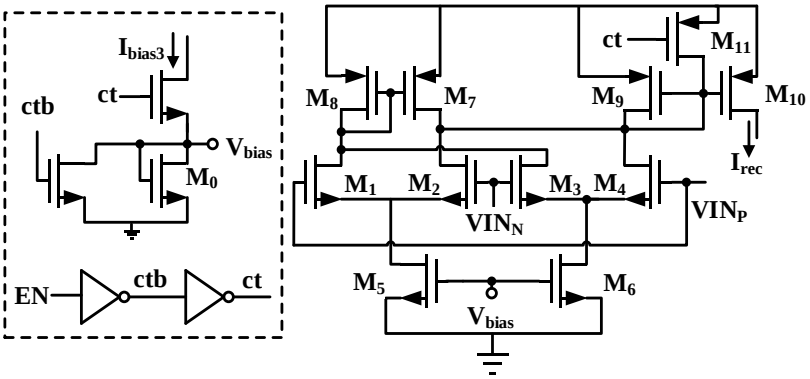
In [12], a limiting amplifier is a differential one with a gain of 10dB and 250μA at a 1.8 V supply. Yet, this design is not efficient because of a complex circuit structure. As shown in Fig. 6(a), the proposed design adopts a two-stage amplifier as the fixed gain stage. The circuit outlined by dotted lines provides the bias voltage (V_{bias}), which is generated by I_{bias1} through a diode connected transistor M_0. The source and drain terminals of M_9 and M_{10} are connected together to act as bypass capacitors. The proposed rectifier circuit [3, 5, 11] is drawn in Fig. 6(b), where the unbalanced source-coupled differential pairs rectify the input signals. The transistor sizes of M_2 and M_4 are k (k>1) times of M_1 and M_3. When there is no input signal, the output current I_{rec} reaches its peak value. The output current I_{rec} is expressed as

$$I_{\mathrm{rec}} = (I_{D2} + I_{D4}) - (I_{D1} + I_{D3}) \qquad (1)$$

Here I_{D1}, I_{D2}, I_{D3}, I_{D4} are drain current of M_1, M_2, M_3, M_4. This proposed rectifier circuit exhibits good linearity, full-wave rectification, and insensitivity to process variation.



(a)



(b)

Fig. 6. (a) Proposed limiting amplifier circuit, and (b) Proposed rectifier circuit

B. DC offset cancellation

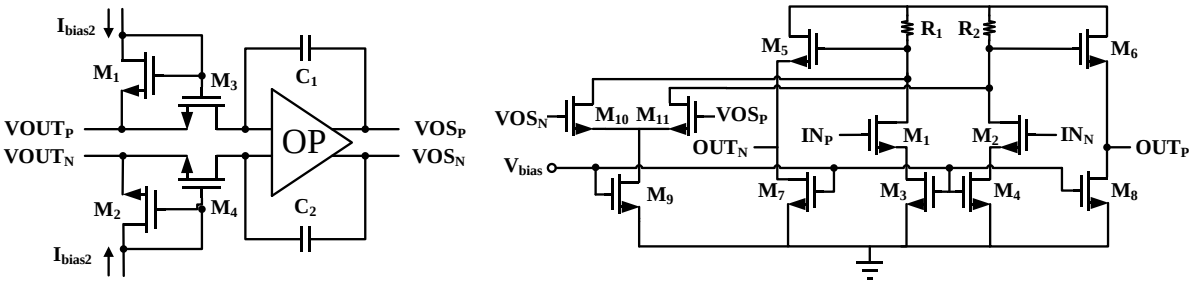
In a limiting amplifier, offset cancellation is essential to eliminate any offset due to device mismatch. An offset cancellation usually consists of an LPF and an offset subtractor. An external passive LPF is used in [4-6]. In [10-11], the use of AC-coupling prevents DC offset from propagating along the amplifier chain. A common drawback of these prior works is the use of large resistor or capacitor, which increases settling time of an RSSI circuit and requires extra chip area. The closed loop gain H_{closed} and low cut-off frequency, ω_L is expressed as [21]

$$H_{\text{closed}}(s) = \frac{A}{1+AF} = \frac{\text{A}_\text{f}\text{A}_0^\text{N}(\omega_0+s)}{(\text{A}_\text{f}\text{A}_0^\text{N}+1)\omega_0+s} \quad (2) \qquad \omega_L \approx A_f A_0^N \omega_0 \quad (3) \qquad \omega_0 = \frac{1}{\text{C}_\text{f}\text{R}_\text{f}} \quad (4)$$

Here, A_f and A_0 are the gains of offset subtractor and limiting amplifier, respectively, N is the stages of limiting amplifiers covered in the DCOC, ω_0 is the -3dB frequency of external passive LPF. In Rx, the input signal frequency to the RSSI circuit is 5MHz. From the equation (4), the required resistance R_f and capacitance C_f are large. In the proposed RSSI design, we utilize an active LPF to decrease the size of capacitance and resistance. Based on the fundamental circuit analysis, the input-referred offset voltage is approximated as

$$VO_{OS} = \frac{\text{A}}{1+\text{A}\beta} VI_{OS} \cong \frac{VI_{OS}}{\beta} \quad (5)$$

Here VO_{OS} and VI_{OS} are the output-referred and input-referred offsets of the RSSI circuit, β is the gain of the LPF, and A is the total gain of the limiting amplifier [9]. As the gain of an active LPF is much higher, the output-referred offset is much less.



(a) (b)

Fig. 7. (a) proposed LPF circuit (b) offset subtractor

Fig. 7(a) depicts the proposed LPF circuit. M_3 and M_4 work in the deep linear region as resistors. Fig. 7(b) shows an offset subtractor, whose inputs are the outputs of the LPF circuit. Fig. 8(a) shows the frequency response, where a -3dB bandwidth of 60Hz is observed. Fig. 8(b) shows the frequency response of the limiting amplifier, whose gain is 46dB and bandwidth is from 170 kHz to 16MHz. The achieved 67dB dc offset suppression effectively rejects low-frequency signals.

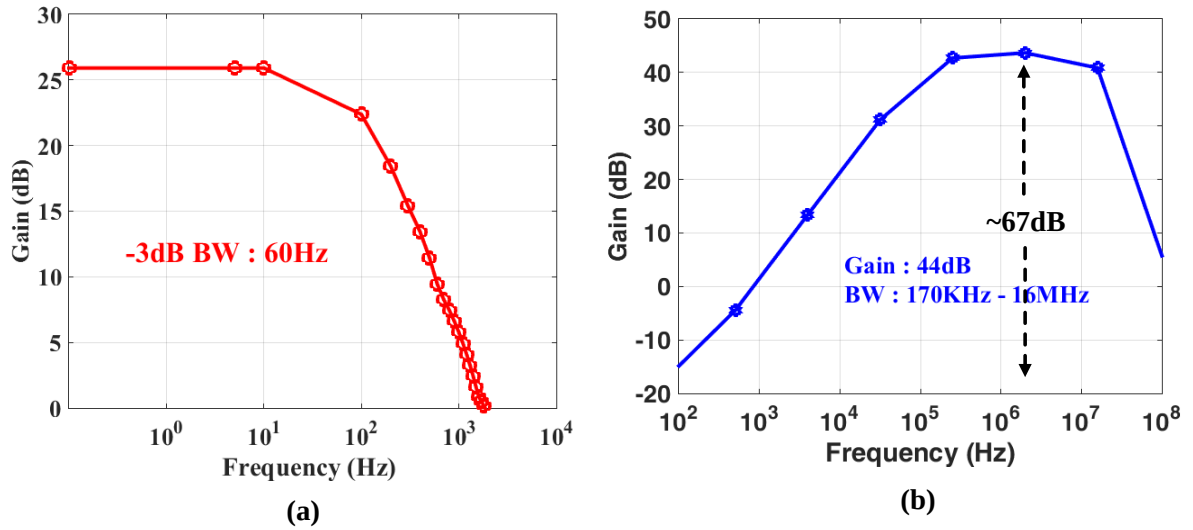


Fig. 8. Frequency response of (a) the active LPF, and (b) the limiting amplifier

C. I-V conversion circuit

In [3-5], the total output current of rectifiers is filtered by a first-order passive LPF, which results in long settling time and large die area. In Fig. 9, the proposed I-V conversion circuit of current to voltage is shown. To solve the above issues, we design an on-chip active LPF to replace the external passive LPF. The required resistance and capacitance are decreased, as well as transient response time. The output current I_{RSSI} is shown as

$$I_{RSSI} = I_{D1} + I_{D2} - I_{rec} \qquad (10)$$

I_{rec} is the total current from the three stages full-wave rectifiers. I_{D1} and I_{D2} are drain currents of M_1 and M_2. I_{bias5} is provided by the common bias generator. The output voltage (V_{RSSI}) is proportional to the input power.

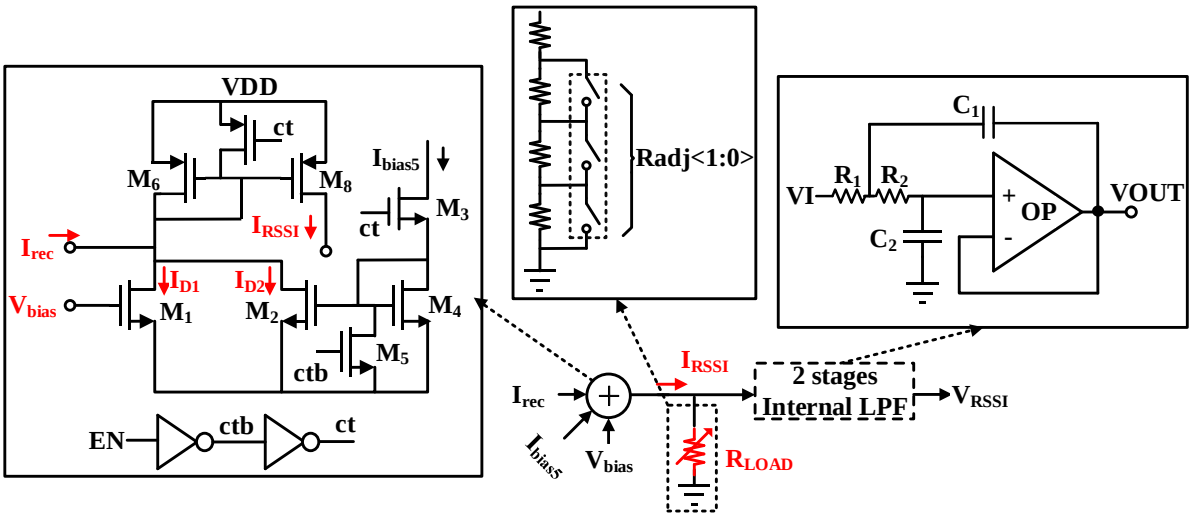


Fig. 9. Proposed I-V conversion circuit

D. Calibration

Process variation affects the circuit performance, such as dynamic range and output voltage range. We integrated two calibration schemes. First, Fig. 10 is the bias generator, where the bias current is controlled by I_{adj}<4:0> to turn on/off current mirrors. Fig. 11(a) plots the simulation results of RSSI output voltage and error versus I_{adj}. Second, the load resistor (R_{LOAD}) is controlled by the digital signal R_{adj}<1:0>. Fig. 11(b) plots the simulation results of RSSI output voltage and error versus R_{adj}. Fig. 12 shows the corner simulation results of RSSI output voltage before and after calibration. We can see that the RSSI variation for three cases of process corners and temperatures are reduced from 2.5dB to 1dB with calibration.

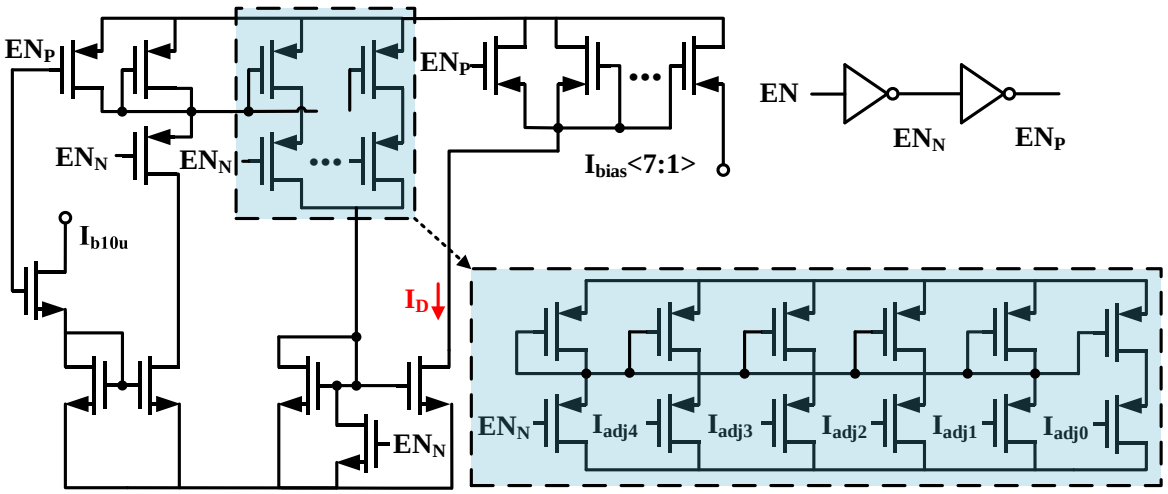
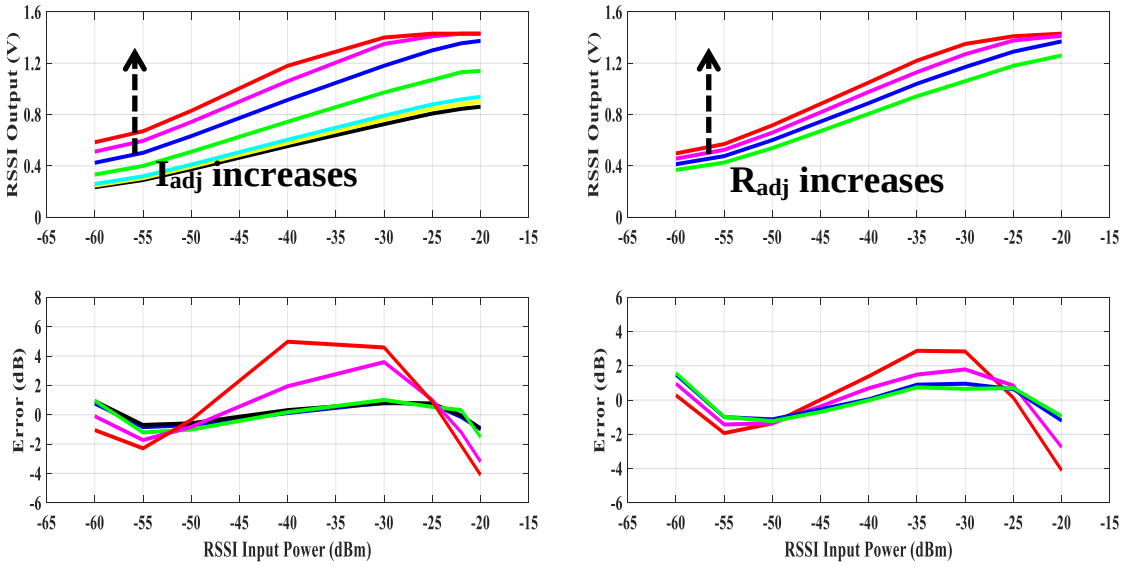
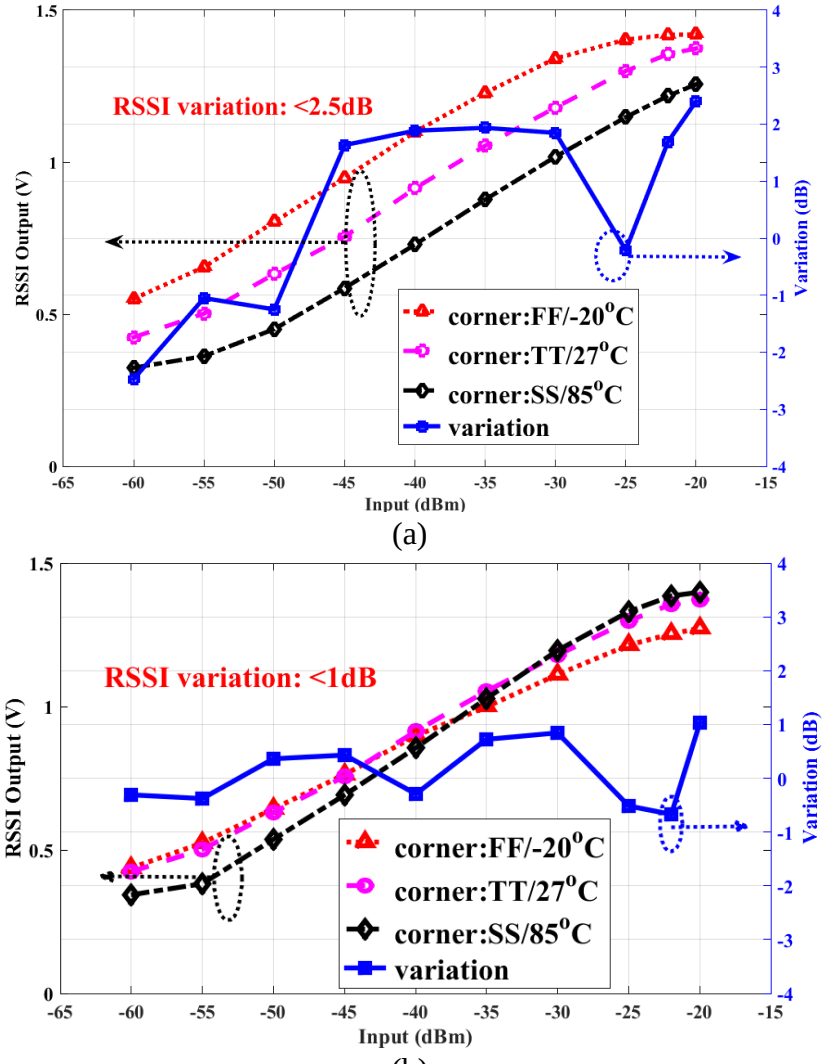


Fig. 10. Bias generator



(a) (b)

Fig. 11. RSSI output and error versus (a) I_{adj} and (b) R_{adj}



(a)

(b)

Fig. 12. (a) Corner simulation results of RSSI output (a) before and (b) after calibration

E. SAR ADC

We propose an 8-bit successive approximation register (SAR) analog-to-digital converter (ADC), in which the logic control circuit, comparators, and capacitive reference network are main sources of power consumption. In the literature, several energy-efficient methods [13-16] have been presented to reduce the switching energy of SAR ADCs. The number of conversion bits can be adjusted to balance between the area, power, conversion rate, and accuracy [18-19]. In [18], a 10-bit SAR ADC is implemented with a 5-bit DAC, and consumes 4.4 µW at a 0.5V supply voltage. In contrast to conventional 10-bit SAR ADCs, the total capacitance can be reduced by more than 96%. In [19], a 5-bit DAC helps to realize an 8-bit SAR ADC with 212nW at a 1V supply voltage. For SAR ADCs, the conversion rate is inversely proportional to the resolution. It is reported [17] that synchronous logic control for the ADCs is not power efficient. The design in [20] achieves a sampling rate of 40MS/s with doubled power consumption. Therefore, asynchronous operation of comparators gets rid of a high-frequency clock and greatly improves the power efficiency [17]. Fig. 13 shows the proposed SAR ADC circuit, where the segmented and V_{CM}-based [16] methods are used to reduce power consumption. Compared to the traditional binary weighting method, the total capacitance is reduced by 50%. In order to reject common-mode noise, a differential architecture is adopted [15]. The simulation results of DNL and INL are shown in Fig. 14(a). The conversion rate is 32.768MHz with a 1.5V supply voltage. The peak values of DNL and INL are -1/1.5 LSB and -1.8/1.8 LSB, respectively. The simulated FFT spectrum shows an input frequency is close to 5MHz as shown in Fig. 14(b). The simulation results of signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 47.633 dB and 62.673dB, respectively. The effective number of bits (ENOB) is found to be 7.62.

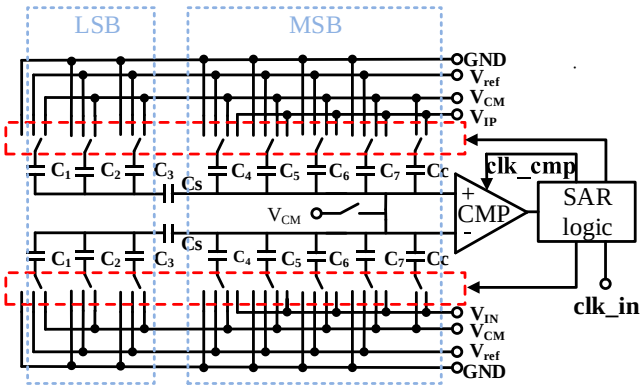
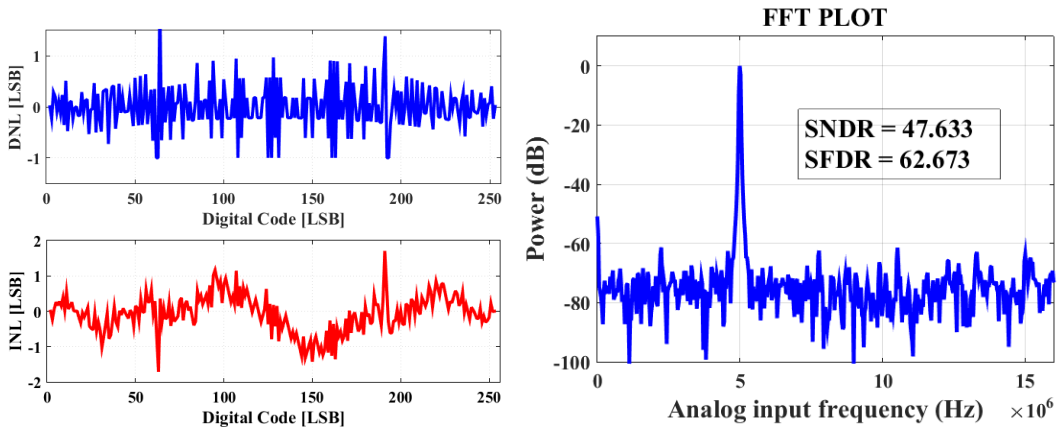


Fig. 13. Proposed SAR ADC Circuit

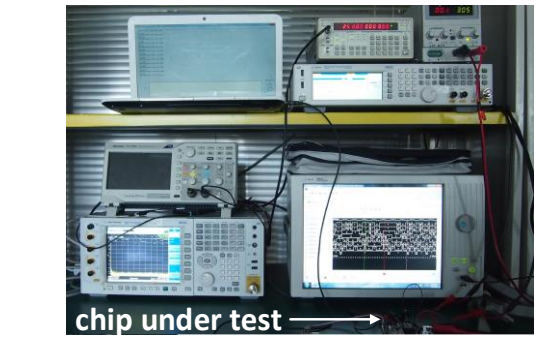


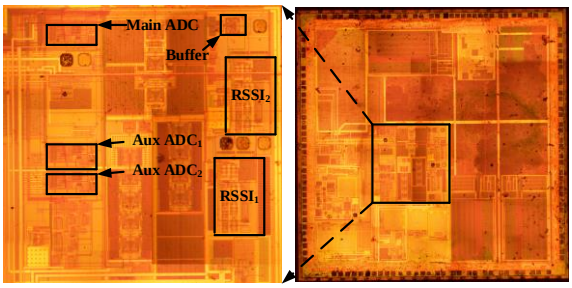
(a) (b)

Fig. 14. Simulation results of DNL and INL, and FFT power plot

IV. Chip Measurement Results and Discussions

The proposed 5.8GHz RF-SoC transceiver is fabricated using a 0.13µm CMOS process. Since there are no specific pads in the chip layout to enable measuring the RSSI circuit alone, we measure the overall circuit performance of the RSSI and SAR ADC. The chip measurement environment and the die micrograph are shown in Fig. 15. The active area of a RSSI is 0.07 mm^2. A QFN package encapsulated the die. Chip measurements were carried out using a dc power supply (*i.e.*, Instek SPS-1230), a signal source generator (*i.e.*, Agilent N5182B), a synthesized clock generator (*i.e.*, Stanford Research System CG635) and a test signal controller. The table in Fig.15 summarizes the performance results of a RSSI and an SAR ADC. In this table, the performance results for RSSI and SAR ARC were measured and simulated, respectively. A RSSI only consumes 0.5mW in active mode, while in sleep mode it consumes 36nW. Due to the use of on-chip active LPFs, the on-off settling time of this design is less than 2µs.





SAR ADC		RSSI	
Area (mm^2)	0.026	Area (mm^2)	0.07
Power (mW)	0.516	Power (on duty) (mW)	0.5
Peak DNL	-1.2 ~ 1.5	Power (off duty) (nW)	36
INL (LSB)	-1.8 ~ 1.8	Accuracy (dB)	< ±1.72
Sampling rate (MHz)	32.77	Dynamic range (dBm)	-60 ~ -20
SNDR (dB)	47.63	On-off settling time (µs)	< 2
SFDR (dB)	62.67		
ENOB (dB)	7.62	Accuracy (dB)	< ±1.72

Fig. 15. Chip measurement environment, micrograph, and performance summary

Fig. 16 plots the measurement results of a RSSI circuit varying with the RSSI input power. We can observe that its linear operation range is from -60dBm to -20dBm. The absolute value of the measurement error is less than 1.72dB. Fig. 17 shows the measurement results of $RSSI_1$ and $RSSI_2$ during the entire chip testing, in which the input power of Rx varies from -90dBm to 0dBm. Under the control of proposed AGC algorithm, appropriate gain settings were adjusted based on the input signal strength. Compared with Fig. 3, the chip measurement curves in Fig. 17 validates the correct operation of the proposed AGC algorithm.

Table III provides a comprehensive comparison of this work with other state-of-the-art designs in the literature. The proposed design demonstrates significant advantages in the overall chip area, power consumption, accuracy, and off-on settling time. The overall input dynamic range achieved is from -86dBm to 0dBm using our AGC algorithm, with an accuracy of ±1.72dB. The transient response is less than 2µs. Compared with these existing designs [3-7] [10] [12], the overall input dynamic range and transient settling time are improved by at least 14.6%, and 300%, respectively. Power consumption and accuracy are also better than most of these existing designs in the literature. All of these design enhancements are due to the proposed new RSSI circuits and system architecture.

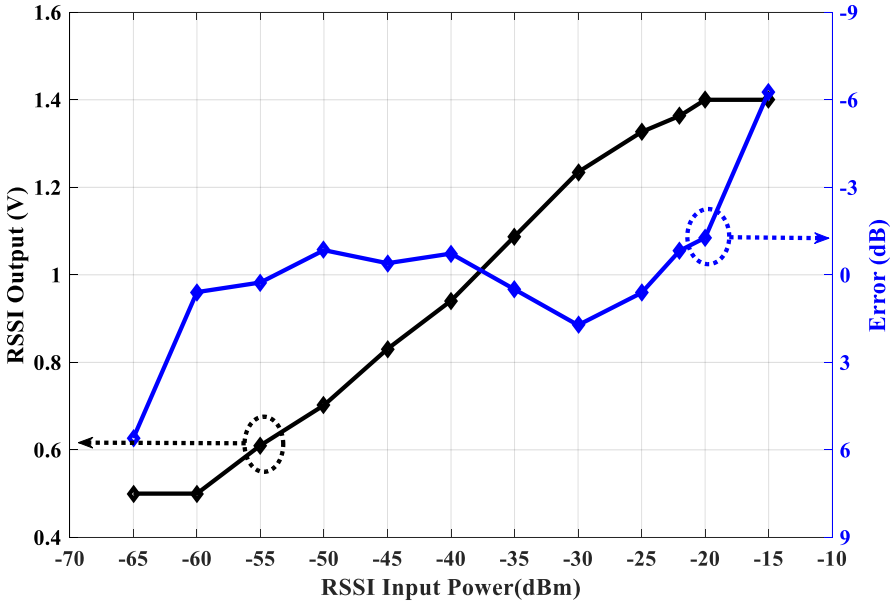


Fig. 16. Measurement results of RSSI output voltage versus RSSI input power

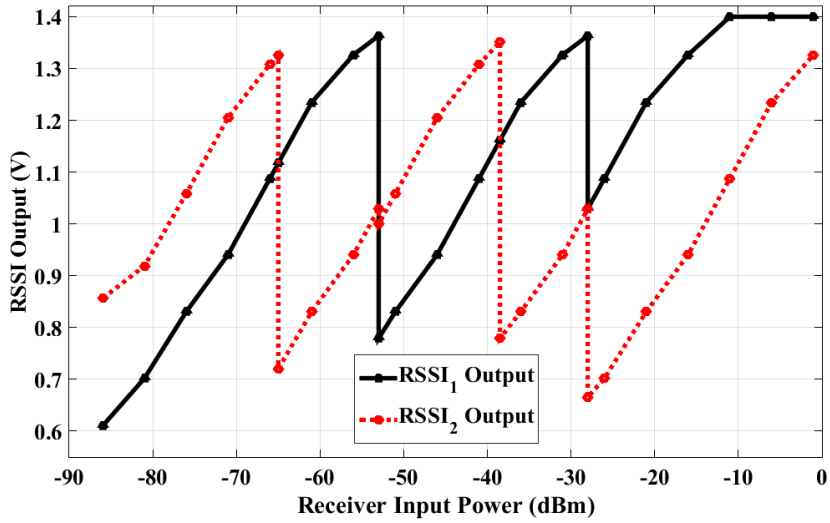


Fig. 17. Measurement results of $RSSI_1$ and $RSSI_2$ during the entire system testing

TABLE II. Comparison of the proposed RSSI with state-of-the-art designs in the literature

Performance Metric	IEEE 2007 [4]	IEEE 2008 [3]	CMCE 2010 [5]	IEEE 2011 [10]	TCSC 2013 [6]	IEEE 2014 [12]	IEEE 2016 [7]	This work
Overall chip area (mm^2)	0.052	0.2	0.11	0.16	0.21	0.6	0.85	0.14
Supply voltage (V)	2.5	1.8	1.8	1.2	1.8	1.8	1.5	1.5
Process (µm)	0.13	0.18	0.18	0.13	0.18	0.18	0.18	0.13
Total power (mW)	9	4.5	3.7	1.8	2.34	4.68	0.54	1
Accuracy (dB)	±1	±2	±1.5	±0.5	±2	±1	±2	±1.72
Overall input dynamic range (dB)	56	75	55	56	70	51	75	86*
Off-on settling time (µs)	N/A	20	N/A	N/A	N/A	N/A	8	2

*this overall dynamic range is achieved by using the proposed algorithm with two RSSIs, each of which has a dynamic range of 40dB.

V. Conclusion

In this paper, a novel RSSI circuit and architecture are proposed and implemented using a 0.13μm CMOS process for a 5.8GHz DSRC ETC system. The removal of one rectifier and external RC components decreases die size and power consumption. Internal active LPFs in the DCOC loop enables full on-chip integration of RSSI circuit, which effectively leads to fast transient response. In order to meet the requirement of the wide input range, two RSSIs with a smaller dynamic range and a proposed algorithm are used instead of one RSSI with a larger dynamic range. Thus, the design complexity of the RSSI circuit is alleviated. Chip measurement results show the overall input dynamic range is 86dB with an accuracy of ±1.72dB, and the transient response is less than 2μs. Compared with the state-of-the-art designs in the literature, the overall input range and transient settling time are improved by at least 14.6%, and 300%, respectively.

VI. ACKNOWLEDGE

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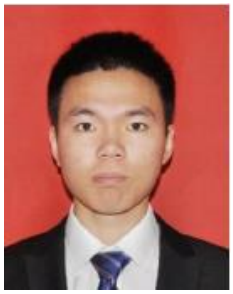

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