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Current Compensation Techniques for Low-voltage High-performance Current Mirror Circuits

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Abstract

This paper presents two current mirror circuits for low-voltage applications. Unlike most current mirrors that use stacked transistors in the output branch to boost the output resistance, the proposed designs use current compensation techniques to achieve high output resistance. By avoiding stacked transistors in the output branch, the minimum output voltages of the proposed circuits are significantly lower compared to those of other current mirror circuits with comparable output resistance. Particularly, the first design emphasizes on reducing the minimum output voltage to an extremely low level of around 20mV. The second design stresses minimizing implementation cost. Compared to a simple current mirror circuit, the second design requires only one additional transistor but boosts the output resistance by more than 10 times. Both circuit analysis and simulations are presented to examine the performance of the proposed designs.

Keywords: Low-voltage, current mirror, current compensation, stability, CMOS circuit

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I. Introduction

Current mirrors (CM) are essential building blocks of analog circuits. Two critical parameters of a CM circuit are its output resistance r_{out} and the minimum output voltage $V_{out,min}$. The latter is also referred to as the CM compliance voltage and is to maintain the accuracy of the input and output current relation. A large r_{out} enhances the accuracy of the CM circuit and helps achieve high amplifier gain when the CM circuit is used as the active load of the amplifier. Meanwhile, a small $V_{out,min}$ improves signal headroom, which is highly desirable in low-voltage design. In general, the efforts to improve one often negatively affects the other, which leads to an increasingly difficult trade-off with the scaling down of circuit supply voltage.

Traditionally, r_{out} of a CM circuit is improved by placing an additional transistor M_3 on top of mirror transistor M_2 as shown in Figure 1 (a). This isolates M_2 from output voltage variations and hence helps stabilize output current I_{out} . By using different methods to generate M_3 gate voltage V_C , this structure has evolved into several well-known CM topologies, including classical cascode, wide-swing cascode, and gate regulated CM circuits [8, 12]. The classical cascode topology biases V_C at the level of $2V_t + 2V_{dsat}$, where V_t is transistor threshold voltage and V_{dsat} is the minimum V_{DS} to keep the transistor in saturation region. Hence, it has $V_{out,min} = V_t + 2V_{dsat}$. The wide-swing cascode topology reduces V_C level to $V_t + 2V_{dsat}$ and subsequently decreases $V_{out,min}$ to $2V_{dsat}$. The gate regulated topology uses an amplifier to form a negative feedback loop that stabilizes M_2 drain voltage to enhance r_{out} . Its $V_{out,min}$ is also about $2V_{dsat}$ due to stacked transistors M_2 and M_3 . In addition to the efforts to boost r_{out} , other techniques have been developed to improve the CM input and output current matching [9, 2] or to reduce the required voltage level at CM input nodes [1, 10]. Nevertheless, these techniques still assume the cascode structure and hence cannot further reduce $V_{out,min}$ below $2V_{dsat}$.

Fig. 1 Techniques to improve CM output resistance

Besides the aforementioned cascode structure, there is an alternative approach to improve CM r_{out} as shown in Figure 1 (b). In the figure, the output branch mirror transistor is modeled by an ideal transistor M_2 in parallel with transistor output resistance r_{o2} . I_{ro} , the current flowing through r_{o2} varies according to the CM output voltage. If a compensation current I_C , which accurately tracks I_{ro} , is added to the CM input branch, then the CM output current I_{out} will not be affected by the variations of the CM output voltage. This method is referred to as current compensation technique in the paper. Since this approach does not require stacked transistors in its output branch, its $V_{out,min}$ can be reduced below $2V_{dsat}$, making it more appealing in low-voltage design.

A CM circuit with current compensation technique is shown in Figure 1 (c) [4, 7, 11]. It uses an amplifier to keep the drain voltages of M_1 and M_2 at the same level. If M_1 and M_2 are matching devices and have the same output resistance, the currents due to the finite output resistance of M_1 and M_2 accurately track each other. Hence, the circuit manifests high r_{out} and has $V_{out,min}$ around V_{dsat} . Once the output voltage is below V_{dsat} , M_1 and M_2 enter linear region and the circuit loses its effectiveness to keep the drain potentials of the mirror transistors equal. Note that this circuit contains a positive feedback loop (amplifier negative input and M_2) and a negative feedback loop (amplifier

positive input and M_1). To make it stable, the impedance at its input node should be larger than that at its output node. A detailed stability analysis for this type of CM circuits is discussed in [11]. Due to the amplifier feedback, the circuit copies its output node voltage to its input node. To achieve high r_{out} and wide voltage swing, its input node should have high impedance and wide swing as well. Such constraints complicate the design of its input source and limit its applications. The CM circuits in [3, 10] implement similar current compensation schemes and avoid the above constraints by using cascode structure in the CM output branch. However, this increases CM $V_{out,min}$ to $2V_{dsat}$ level, making them unsuitable in ultra-low voltage applications.

Table 1 Output resistance and compliance voltage comparison

Types of CM circuits	r_{out}	$V_{out,min}$
Simple CM circuit	r_o	V_{dsat}
Classical Cascode CM	$g_m r_o^2$	$V_t + 2V_{dsat}$
Wide-swing Cascode	$g_m r_o^2$	$2V_{dsat}$
Gate-regulated Cascode [8]	$A g_m r_o^2$	$2V_{dsat}$
Low-voltage Wilson CM [6]	$g_m r_o^2$	$2V_{dsat}$
CM Circuit in [5]	$g_m^2 r_o^3$	$> V_{dsat}$
Current compensation CM circuit in [4, 7]	$-r_{in}^*$	V_{dsat}
Prop. high-perform CM circuit	$A r_o$	$< V_{dsat}$
Prop. ORBCM circuit	$\frac{r_{o4} \cdot r_{o1}}{r_{o4} - r_{o1}}$	V_{dsat}

* r_{in} is the impedance observed at the input node of the CM circuit. The circuit in [4,7] has a negative output resistance.

Table 1 summarizes the achievable r_{out} and $V_{out,min}$ of various CM circuits. In the table, g_m and r_o denote transistor transconductance and output resistance; A is the gain of the amplifier used in the design. Clearly, the $V_{out,min}$ of CM circuits with the stacked structure is about $2V_{dsat}$ or above, with the exception of the circuit in [5], in which one of the stacked transistors operates in linear region. Meanwhile, the current compensation based CM circuits in [4, 7] reduce $V_{out,min}$ to V_{dsat} level, but suffer from several limitations as discussed earlier. This paper presents two low-voltage current compensation based CM circuits whose r_{out} and $V_{out,min}$ are listed in the last two rows of the table. The first design, referred to as high-performance CM circuit, emphasizes on pushing $V_{out,min}$ to an extremely low level that is around 20mV. Unlike the previous low-voltage CM circuit [4, 7], the proposed design does not require the CM input node to have high impedance and wide swing. The second design, referred to as output resistance boosted simple CM circuit (ORBCM), stresses minimizing the implementation cost. It requires only one additional transistor but significantly boosts r_{out} compared to a simple CM circuit. Both circuit analysis and simulations are presented to discuss their design considerations and to demonstrate their superb performance.

The rest of the paper is organized as follows. Section 2 describes the proposed high-performance CM circuit. Its output resistance and stability are also discussed in this section. The ORBCM circuit and its design considerations are presented in Section 3. Circuit simulation results are presented in Section 4 and the paper is concluded in Section 5.

II. Proposed high-performance current mirror circuit

The proposed high-performance CM circuit is shown in Figure 2. It uses a feedback loop consisting of amplifier A1 and transistor M_2 to ensure NMOS mirror transistors M_1 and M_4 have the same drain voltage. Thus, the CM output I_{out} precisely tracks I_{DS4} . Meanwhile, another feedback loop comprised of amplifier A2, transistors M_4 , M_2 and M_3 forces PMOS mirror transistors M_3 and M_5 to have the same drain potential, resulting in $I_{DS3} = I_{DS5}$. Since $I_{DS3} = I_{in}$ and

$I_{DS4} = I_{DS5}$, we have $I_{out} = I_{in}$. To further illustrate how the input and output current relation is enforced by the feedback loops in a dynamic manner, we assume V_{out} increases by ΔV . Then the output of amplifier A1 increases and so does V_{DS4} . This momentarily causes I_{DS4} to increase, mainly due to the finite output resistance of M_4 with the assumption that M_4 gate voltage V_G is not affected yet. The increase on I_{DS4} is then passed to I_{DS3} and subsequently causes M_3 gate voltage V_C to decrease. As a result, amplifier A2 decreases M_1 and M_4 gate voltage V_G to settle the circuit into a new stable state. Thus, the mechanism to realize current compensation can be summarized as follows. When V_{out} increases, so does current $I_{r_{o1}}$, the current flowing through M_1 output resistance r_{o1} . The feedback system reduces the gate voltage of M_1 such that the current reduction due to decreased V_G compensates the increase on $I_{r_{o1}}$.

Fig. 2 Proposed high-performance CM circuit

Fig. 3 Small signal model of the proposed CM circuit

The small signal model of the proposed circuit is shown in Figure 3. Note that frequency compensation capacitors C_{1-3} in Figure 2 are not included in the small signal model. As detailed in Appendix A, the r_{out} of the proposed circuit can be derived as:

$$r_{out} = \frac{1}{\frac{1}{r_{o1}} - \frac{g_{m1}g_{m2}A_1A_2\left(1 + \frac{g_{m5}r_{o5}}{2}\right)}{\left(\frac{1}{r_{o2}} + g_{m2}(A_1 + 1) + g_{mb2}\right)\left(\frac{r_{o4}}{r_{o3}} + g_{m3}r_{o4} + g_{m4}r_{o4}A_2\left(1 + \frac{g_{m5}r_{o5}}{2}\right)\right) + \frac{1}{r_{o3}} + g_{m3} + \frac{1}{r_{o2}}}} \quad (1)$$

where A_1 and A_2 denote the gain of amplifiers A1 and A2. If A_2 is large, the above equation can be approximately simplified as:

$$r_{out} \approx A_1 \cdot r_{o1} \quad (2)$$

The proposed circuit has several advantages over the previous designs [4, 7]. First, mirror transistors M_1 and M_4 are not directly contained in the feedback loop that controls their drain potential. Thus, even if M_1 and M_4 leave saturation region, the feedback loop can still keep their drain voltages at the same level, which allows $V_{out,min}$ of the proposed circuit to be reduced below V_{dsat} . Second, the proposed circuit does not copy the output voltage level to its input node and hence eliminates the requirements of high impedance and wide swing for its input node. This simplifies the CM input driving circuit design and improves current matching.

Since the proposed circuit contains several feedback loops, stability is an important design concern. First, compensation capacitors $C_{1\sim3}$ are used to improve the phase margin of the aforementioned negative feedback loops. These capacitors also perform frequency compensation for amplifiers A1 and A2. Second, there is a positive feedback loop comprised of the positive input of amplifier A1, transistor M_2 , the positive input of amplifier A2, and transistor M_1 . As shown in Appendix B, its open loop gain G_{OL1} can be derived as:

$$G_{OL1} \approx \left(\frac{A_1}{1 + A_1}\right) \frac{\left(1 + \frac{g_{m5}r_{o5}}{2}\right) \frac{g_{m1}(r_{o1}||r_L)}{r_{o4}g_{m3}} A_2}{1 + \left(1 + \frac{g_{m5}r_{o5}}{2}\right) \frac{g_{m4}}{g_{m3}} A_2} \quad (3)$$

where r_L represents the CM circuit output load resistance. Since $g_{m1} = g_{m4}$, $r_{o1} = r_{o4}$, $A_1 \gg 1$, and $\left(1 + \frac{g_{m5}r_{o5}}{2}\right) \frac{g_{m4}}{g_{m3}} A_2 \gg 1$, the above equation can be simplified as:

$$G_{OL1} \approx \frac{r_{o1}||r_L}{r_{o4}} < 1 \quad (4)$$

This indicates that the positive feedback loop gain is always smaller than 1 and hence it does not undermine the stability of the proposed circuit.

III. Output resistance boosted simple current mirror circuit

The proposed ORBCM circuit strives to improve CM output resistance with minimized hardware overhead. Compared to the simplest CM circuit in Figure 4 (a), the proposed circuit depicted in Figure 4 (b) requires only one additional transistor M_3 . It implements compensation current I_C by taking advantage of the output resistance of the CM driving device M_4 . Also, transistor M_3 functions as a source follower, thus the drain potential of M_4 tracks the voltage variation at the output node. Assuming V_{out} experiences a change of ΔV , then the current flowing through the output resistance of M_1 changes by $\frac{\Delta V}{r_{o1}}$. Meanwhile, ΔV is propagated to the drain terminal of M_4 since V_{GS3} is constant thanks to the relatively stable I_{DS3} . Thus, the change on the current flowing through the output resistance of M_4 is $\frac{\Delta V}{r_{o4}}$. If $r_{o1} = r_{o4}$, compensation current I_C will completely cancel the variation on the current flowing through the output resistance of M_1 , thus boosting the output resistance of the CM circuit.

The small signal model of the ORBCM circuit is shown in Figure 4 (c). As described in Appendix C, its output resistance can be derived as:

$$r_{out} = \frac{1}{\frac{1}{r_{o1}} - \frac{g_{m3} \cdot g_{m1} \cdot r_{o3}}{[r_{o3} + r_{o4} + r_{o3} \cdot r_{o4}(g_{m3} + g_{mb3})] \left[\frac{1}{r_{o2}} + g_{m2} \right]} + 1} \quad (5)$$

If $g_{m1} = g_{m2}$, $g_{m2} \gg \frac{1}{r_{o2}}$ and $g_{m3} \gg g_{mb3}$, the above expression can be simplified as:

$$r_{out} \approx \frac{1}{\frac{1}{r_{o1}} - \frac{1}{r_{o4}}} = \frac{r_{o4} \cdot r_{o1}}{r_{o4} - r_{o1}} \quad (6)$$

It shows that r_{out} can be significantly improved if $r_{o1} \approx r_{o4}$. Since M_1 and M_4 are different types of transistors, achieving exact matching between r_{o1} and r_{o4} may not be realistic. However, as long as r_{o1} and r_{o4} are reasonably close, the proposed CM circuit will have much higher r_{out} than the simple CM circuit and this is achieved with using only one additional transistor. Although process variations will affect the matching between r_{o1} and r_{o4} , simulation results demonstrate that the proposed design retains its high r_{out} advantage at the presence of process variations. Finally, if $r_{o1} > r_{o4}$, the ORBCM circuit will manifest a negative output resistance, which can be tolerated in various applications, e.g. the CM circuit functioning as the tail current source of differential amplifiers. However, if a negative resistance is undesirable, r_{o4} can be designed to be larger than r_{o1} with adequate design margin.

Fig. 4 Proposed ORBCM circuit and its small signal model

The ORBCM circuit also contains a positive feedback loop comprised of two stages. The first stage is a source degenerated common source (CS) amplifier with M_3 as the amplification device and diode-connected M_2 as the active load. The second stage is the CS amplifier with amplification device M_1 . Assume r_L is the load resistance at the ORBCM circuit output. The loop gain of the positive feedback can be derived as:

$$G_{OL2} \approx \frac{g_{m1}}{r_{o4}g_{m2}}(r_{o1}||r_L) \approx \frac{r_{o1}||r_L}{r_{o4}} < 1 \quad (7)$$

Therefore, the positive feedback will not cause instability in practical applications.

IV. Circuit simulation results

The two proposed circuits are designed using a 0.13 μ m CMOS technology and operate with a single 1.2V power supply. Circuit simulations show that the proposed high-performance CM circuit can simultaneously achieve high r_{out} and extreme low $V_{out,min}$ that is about 20mV. Its stability is also validated by simulation results. For the ORBCM circuit, simulation results demonstrate that it improves r_{out} by more than 10 times compared to a simple CM circuit.

Simulations are also conducted to study the impact of process variations and to demonstrate the advantages of using the ORBCM circuit in amplifier design.

A. Proposed high-performance CM circuit

In the design of the proposed high-performance CM circuit, two-stage topologies are used for amplifiers A1 and A2 to achieve moderate gain and relatively large output swing. If the mirror transistors have large size, the amplifier output swing requirement will be relaxed and, subsequently, single-stage differential amplifiers can be used. The amplifier schematics are given in Figure 5 and the types of amplifier input devices are selected based on their common mode input range requirements. Transistor sizes used in the design are listed in Table 2 and the compensation capacitors are selected as: $C_1 = 0.1 \text{ pF}$, $C_2 = 0.1 \text{ pF}$, and $C_3 = 0.2 \text{ pF}$. The attained gains for amplifiers A1 and A2 are 31 and 42, respectively. The CM circuit is designed for an output current of $6 \mu\text{A}$.

Fig. 5 Amplifier circuits used in the high-performance CM circuit

Table 2 Transistor sizes of the high-performance CM circuit

Device	Channel width/ length	Device	Channel width/ length
M1, M4	$3\mu\text{m}/120\text{nm}$	M12	$540\text{nm}/360\text{nm}$
M2	$1.44\mu\text{m}/120\text{nm}$	M13	$600\text{nm}/120\text{nm}$
M5, M3	$600\text{nm}/120\text{nm}$	M14, M15	$420\text{nm}/120\text{nm}$
M6, M7	$600\text{nm}/120\text{nm}$	M16, M17	$3\mu\text{m}/120\text{nm}$
M8, M9	$360\text{nm}/120\text{nm}$	M18	$180\text{nm}/120\text{nm}$
M10	$320\text{nm}/120\text{nm}$	M19	$1.26\mu\text{m}/360\text{nm}$
M11	$540\text{nm}/120\text{nm}$	C1/C2/C3	$0.1/0.1/0.2 \text{ pF}$

For comparison purposes, the CM circuits in [4, 5] are also designed and simulated using the same CMOS technology. The schematic of the circuit in [4] is shown in Figure 1 (c). It uses the same mirror transistor sizes as that of M_1 and M_4 in the proposed design and amplifier A1 is used in the feedback loop. The transistor sizes of the circuit in [5] are selected following the techniques in [5] with targeted output current of $6 \mu\text{A}$. Figure 6 plots the output currents of the three CM circuits. If the compliance voltage is selected as the output level at which the output current differs from the ideal value by 1%, the compliance voltages of the proposed circuit and the designs in [4] and [5] are 20 mV, 53mV, and 117 mV, respectively. The relative current errors of the three circuits are plotted in Figure 7. It shows the three designs approximately achieve the same level of accuracy. With a $1 \text{ K}\Omega$ load resistance, simulations are also performed to compare the noise performance of the three circuits. The output white noises of the proposed circuit and the designs in [4] and [5] are $6.43 \text{ pA}/\sqrt{\text{Hz}}$, $6.16 \text{ pA}/\sqrt{\text{Hz}}$ and $5.3 \text{ pA}/\sqrt{\text{Hz}}$, respectively. It shows the proposed technique does not significantly affect the noise performance of the CM circuit.

Fig. 6 Output currents of the proposed high-performance CM circuit and reference designs in [4, 5]

Fig. 7 Relative output current errors of the proposed high-performance CM circuit and reference designs in [4, 5]

Fig. 8 Simulated open loop gain of the positive feedback path

Figure 8 shows the simulated open loop gain G_{OL1} of the aforementioned positive feedback path. In simulation, the loop is cut at amplifier A1 positive input, to which an AC signal is injected for AC analysis. The differential amplifier depicted in Figure 10 serves as the load of the CM circuit in simulation. Due to the small load resistance r_L , G_{OL1} is below -20dB. Using an active load with an output resistance similar to that of M1, G_{OL1} is still below -6dB, which confirms the stability analysis in Section II.

B. Proposed ORBCM circuit

Both the proposed ORBCM circuit and the simple CM circuit in Figure 4 (a) are designed with $I_{out} = 6 \mu A$. The two circuits have the same transistor sizes, as shown in Table 3, and only differ by that the ORBCM circuit has an extra transistor M_3 . The simulated output currents of the two circuits are compared in Figure 9. Clearly, the output current of the ORBCM circuit is much more stable and the two circuits approximately have the same $V_{out,min}$, which is about the level of V_{dsat} . When the output voltage is at 600mV, the r_{out} of the ORBCM and simple CM circuits are 3.5M Ω and 310k Ω , respectively. This represents 11 times improvement by the proposed technique. Simulation also reveals that $r_{o1} = 380 K\Omega$ and $r_{o4} = 415 K\Omega$ in the aforementioned conditions. According to Equation 6, r_{out} of the ORBCM circuit is about 4.5M Ω , which is reasonably close to the value obtained from simulation.

Table 3 Transistor sizes of the current mirror circuit

Device	Channel width/ length
M1, M2	1.2 μm /360nm
M3	4.8 μm /120nm
M4	9.6 μm /240nm

Fig. 9 Output current of the simple CM and ORBCM circuit; a: simple CM circuit; b: ORBCM circuit

Since the r_{out} of the ORBCM circuit strongly depends on the matching between r_{o1} and r_{o4} , Monte Carlo (MC) simulations are conducted to study how process variations and device mismatches affect the proposed technique. The histogram of the ORBCM r_{out} from 1000 MC simulations is shown Figure 10. Note that the three largest r_{out} values, 66M Ω , 68M Ω and 605M Ω are significantly higher than the rest of the values and are not included in the plot in order to avoid overstressing the x-axis of the plot. The r_{out} mean and standard deviation values are 4.3M Ω and 2.8M Ω , respectively. This shows that r_{out} has a wide distribution. In many scenarios, the requirement for CM output resistance is to be larger than, rather than tracking, a target value. Thus, the wide r_{out} distribution can be tolerated as long as the majority of the distribution is larger than the target value. The minimum r_{out} obtained from the 1000 MC simulations is 980K Ω , which is still 2.5 times larger than the output resistance of the simple CM circuit. Also, 99% of the obtained r_{out} values are larger than 1.5M Ω , which is almost four times of the output resistance of the simple CM circuit. This demonstrates that the proposed technique remains effective at the presence of process variations and device mismatches.

With a 1K Ω load resistance, the output white noise of the ORBCM and simple CM circuits are 5.42 $pA/\sqrt{Hz}$ and 5.62 $pA/\sqrt{Hz}$, respectively. Simulations are also conducted to show the CMRR (common mode rejection ratio) of a differential amplifier can be improved by using the ORBCM circuit as its tail current source. The amplifier schematic and its transistor sizes are shown in Figure 11. For comparison purposes, both the ORBCM circuit and simple CM circuit are used in the study. Figure 12 compares the obtained CMRRs at a common mode input level of 600mV. It shows that about 18dB improvement, from 53dB with the simple CM circuit to 71dB with the ORBCM circuit, is achieved by adding only one extra transistor in the design.

Fig. 10 Histogram of the ORBCM circuit r_{out}

Fig. 11 Amplifier design for CMRR comparison

Fig. 12: Amplifier CMRR using the ORBCM or the simple CM circuit as its tail current source

V. Conclusions

This paper presents two low-voltage CM circuit designs using current compensation techniques to improve CM output resistance. Unlike most existing CM circuits that rely on stacked transistors in the output branch to stabilize the drain potential of the output device, the proposed circuits place only one transistor in their output branches, which helps reduce output compliance voltage. In the first proposed circuit, amplifier based feedback loops are used to achieve current compensation. Additionally, the mirror devices are not contained in the critical path of the feedback, allowing the mirror devices to operate in deep linear region without significantly affecting the effectiveness of the feedback loops. This enables the proposed design to achieve extremely compliance voltage at the level of 20 mV, which to our knowledge is the lowest compliance voltage of any implementation reported in literature. In the second design, the current compensation is achieved by copying the voltage variations at the CM Output node to its input node and matching the output resistance of the output device with the output resistance of its driver circuit. This design only requires one addition transistor compared to a simple CM circuit but can significantly improve CM output resistance. The effectiveness of the proposed design at the presence of process variation and device mismatches is verified via MC simulations. Thanks to their low compliance voltage and high output resistance, the proposed designs are suitable for various low-voltage applications.

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Appendix A

This appendix derives the output resistance of the proposed high-performance CM circuit. From the small signal model shown in Figure 3 we have:

$$I_{out} = \frac{V_{out}}{r_{o1}} + g_{m1}V_G \quad (8)$$

$$I_c = \frac{V_D}{r_{o4}} + g_{m4}V_G \quad (9)$$

$$I_c = \frac{V_C - V_D}{r_{o2}} + g_{m2}(V_{A1} - V_D) - g_{mb2}V_D \quad (10)$$

$$I_c = -\frac{V_C}{r_{o3}} - g_{m3}V_C \quad (11)$$

$$V_{A1} = (V_{out} - V_D)A_1 \quad (12)$$

$$V_G = V_C(1 + g_{m5} \cdot (r_{o5} || r_{in}))A_2 = (V_C - V_R)A_2 \quad (13)$$

Assuming $r_{in} \approx r_{o5}$, V_G can be approximated by:

$$V_G = V_C \left(1 + \frac{g_{m5} \cdot r_{o5}}{2}\right) A_2 \quad (14)$$

From the above equations, I_{out} can be solved as:

$$I_{out} = \frac{V_{out}}{r_{o1}} - \frac{g_{m1}g_{m2}A_1A_2 \left(1 + \frac{g_{m5}r_{o5}}{2}\right) \cdot V_{out}}{\left(\frac{1}{r_{o2}} + g_{m2}(A_1 + 1) + g_{mb2}\right) \left(\frac{r_{o4}}{r_{o3}} + g_{m3}r_{o4} + g_{m4}r_{o4}A_2 \left(1 + \frac{g_{m5}r_{o5}}{2}\right)\right) + \frac{1}{r_{o3}} + g_{m3} + \frac{1}{r_{o2}}} \quad (15)$$

Thus,

$$r_{out} = \frac{1}{\frac{1}{r_{o1}} - \frac{g_{m1}g_{m2}A_1A_2 \left(1 + \frac{g_{m5}r_{o5}}{2}\right)}{\left(\frac{1}{r_{o2}} + g_{m2}(A_1 + 1) + g_{mb2}\right) \left(\frac{r_{o4}}{r_{o3}} + g_{m3}r_{o4} + g_{m4}r_{o4}A_2 \left(1 + \frac{g_{m5}r_{o5}}{2}\right)\right) + \frac{1}{r_{o3}} + g_{m3} + \frac{1}{r_{o2}}}} \quad (16)$$

Appendix B

This appendix derives the open loop gain of the positive feedback path in the proposed high-performance CM circuit. Assuming V_{GS2} is approximately constant, V_D can be approximated by:

$$V_D = \left(\frac{A_1}{1 + A_1}\right) V_{A1+} \quad (17)$$

where V_{A1+} is the non-inverting input of amplifier A1. Also, V_C as a function of V_D and V_G can be approximated by:

$$V_C = -V_D \frac{1}{r_{o4}g_{m3}} - V_G \frac{g_{m4}}{g_{m3}} \quad (18)$$

where V_G is given in Equation 14. From Equations 14, 17, 18, we can solve V_G as:

$$V_G = - \frac{\frac{V_{A_{1+}}}{r_{o4}g_{m3}} \left(\frac{A_1}{1+A_1} \right)}{\frac{1}{\left(1 + \frac{g_{m5}r_{o5}}{2}\right)A_2} + \frac{g_{m4}}{g_{m3}}} \quad (19)$$

Finally, transistor M_1 and the CM load with output resistance r_L form a common source amplifier with the gain of $-g_{m1}(r_{o1}||r_L)$. Thus, the open loop gain defined as $G_{OL1} = \frac{V_{out}}{V_{A_{1+}}}$ is:

$$G_{OL1} \approx \left(\frac{A_1}{1+A_1} \right) \frac{\left(1 + \frac{g_{m5}r_{o5}}{2}\right) \frac{g_{m1}(r_{o1}||r_L)}{r_{o4}g_{m3}} A_2}{1 + \left(1 + \frac{g_{m5}r_{o5}}{2}\right) \frac{g_{m4}}{g_{m3}} A_2} \quad (20)$$

Appendix C

This appendix derives the r_{out} of the ORBCM circuit. From the small signal model in Figure 4 (c), we have:

$$I_{out} = \frac{V_{out}}{r_{o1}} + g_{m1}V_1 \quad (21)$$

$$-I_c = \frac{V_1}{r_{o2}} + g_{m2}V_1 \quad (22)$$

$$I_c = \frac{V_1 - V_2}{r_{o3}} + g_{m3}(V_{out} - V_2) - g_{mb3}V_2 \quad (23)$$

$$I_c = \frac{V_2}{r_{o4}} \quad (24)$$

Solving for I_{out} from the above equations and subsequently for r_{out} we find the expression:

$$r_{out} = \frac{1}{\frac{1}{r_{o1}} - \frac{g_{m3} \cdot g_{m1} \cdot r_{o3}}{[r_{o3} + r_{o4} + r_{o3} \cdot r_{o4}(g_{m3} + g_{mb3})] \left[\frac{1}{r_{o2}} + g_{m2} \right] + 1}} \quad (25)$$