Effects of Deposition Process on Poly-Si Microscale Energy Harvesting Systems: A Simulation Study

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Effects of Deposition Process on Poly-Si Micro-scale Energy Scavenging Systems

Elif S. Mungan, Chao Lu, Chih-Hsiang Ho and Kaushik Roy, Fellow, IEEE

Abstract—In this paper, the feasibility of a low temperature polysilicon (LTPS) micro-scale energy harvester for a wireless sensor node is investigated. For that purpose, two device level models for the LTPS solar cell and thin film transistors (TFTs) are proposed and employed in system level evaluation of an energy harvesting system. The results of our analysis indicate that (i) the maximum power operating point for the solar cell is different when connected to a lossy power converter, (ii) increasing the average grain size (GS) of the LTPS film can reduce the circuit area by 20 times while increasing the output power by 6%, (iii) the performance of the wireless sensor node is limited by the TFT performance for an LTPS process with high trap density (NT).

Index Terms—energy harvesting, grain boundaries, numerical simulations, optimization, photovoltaic cells, statistical analysis, thin film transistors.

I. INTRODUCTION

FROM patient monitoring [1] to agricultural management [2] or space weather visualization [3] to assessing the condition of a bridge [4], many applications call for self-sufficient systems when battery replacement is not a favorable option. These systems can be implemented with wireless sensor networks which are created by deploying a vast number of sensors that communicate with a central processor making the decisions. To achieve self-sufficiency, the wireless sensor networks are required to harvest energy such as solar, thermal, piezoelectric or radio-frequency energies which are readily available in the ambient environment [5]. Among these available sources, solar energy is the most promising one due to its high power density -- in the mW/cm² range for outdoor, and in the μW/cm² range for indoor applications [6].

In a wireless sensor node as illustrated in Fig. 1, the power consumed by the sensing and communication units are provided by the micro-scale energy harvesting unit that utilizes a solar cell as the energy source. Due to the low output voltage of the solar cell (V_{PV}), it needs to be converted to the required system voltage (V_{VDD}) to operate the sensors and transmit the obtained data to the central processor. This conversion is handled by a DC-DC power converter whose switching frequency (f_{SW}) is determined by a control circuitry that makes sure the solar cell is biased at the optimum operating point under different light intensities. The harvested energy is stored in energy buffer that can be a rechargeable battery or a supercapacitor.

Since wireless sensor networks employ large numbers of sensor nodes, the nodes are required to be compact, low cost and consume low power. The cost of an integrated circuit can be reduced by reducing the thermal budget of the deposition process. Hence, unlike the conventional approach, in this work the micro-scale energy harvester is envisioned to be integrated on a glass substrate using low temperature polysilicon (LTPS) technology. On the other hand, reducing the thermal budget causes the deposited materials to be polycrystalline (poly). These materials are composed of crystalline regions with different orientations (grains) and defective regions where the grains meet (grain boundaries (GBs)). The traps along GBs degrade the performance of the devices fabricated with this process and therefore introduce trade-offs for the system design in terms of system area, speed and power consumption. This degradation, however, can be tolerated for wireless sensor networks since the duty cycles can be around 1% [6].

The aim of this work is to make sure that the LTPS process can be used to fabricate the wireless sensor node in Fig. 1 despite the degradation due to GBs. To achieve this goal, one should be able to model the implications of GBs on the performance of the fundamental building blocks of the system. For this purpose, device level models are proposed for the polysilicon solar cell and thin film transistor (TFT), which are the building blocks of the proposed energy source and integrated circuits, respectively. Using compact models, the performance of the proposed devices are assessed at the circuit level and the overall system is optimized as the solar cell array and the power conditioning units are co-optimized. By

Fig. 1 Signal flow between the operating units of a wireless sensor node
following this holistic approach, the effects of process parameters namely silicon thickness ($t_{Si}$), average grain size (GrS) and GB trap density ($N_T$) on the performance of these devices, circuits and the system are investigated. Unlike the conventional approach, our holistic approach provides more insight, gives more control over the process and indicates the design tradeoffs that are not visible when each building block is studied in isolation.

The rest of this paper is organized as follows: the device-level model proposed for the LTPS solar cell is discussed in Section II, followed by the model for the LTPS TFT in Section III. The performance of the TFT model is assessed in a power converter circuit in Section IV. The building blocks of a wireless sensor network (the energy source, the power converter and the peripheral circuitry) are put together to study the system performance and sensitivity to process parameters in Section V. Finally, the conclusions are drawn in Section VI.

II. SOLAR CELL MODELING

As the power source of the system on glass, the solar cell device structure in Fig. 2b was proposed previously in [7]. Since the aim of this work is to use the same process technology for the solar cell and TFTs used for the power converter and application units, the range for $t_{Si}$ is kept below 1 μm. Using a classical device structure in which anode and cathode are placed on top and bottom of the cell would be problematic for thin devices since it could have caused shunting problem during contact formation [8]. Therefore, the proposed cell structure is kept similar to a TFT as it can be seen from Fig. 2b.

Previously in [7], the distance between n+ and p+ doped Si regions ($W_{SC}$) was assumed to be equal to the GrS of a process such that the maximum number of GBs in the channel is limited to one. This requires very short $W_{SC}$ which increases the process complexity and cost. To study the trade-off between performance and cost, the solar cell model in [7] is improved such that it can simulate device structures with multiple GBs, $W_{SC}$ and $t_{Si}$ in a faster fashion. This is achieved by solving 1D drift-diffusion equations using the Newton’s iteration scheme for the structure in Fig. 2b [9].

The optical generation profiles used to model solar cells with different $t_{Si}$s were reported in [10]. GBs are modeled as 4nm-wide regions with $N_T$ and the energy levels indicated in [11]. Furthermore, GBs are assumed to be unidirectional and orthogonal to the current flow while the illumination is assumed to be at standard terrestrial conditions (AM 1.5) [12].

The results of our analysis are compared with 2D simulation results obtained for the same structure in a commercial drift-diffusion solver, Sentaurus [13]. The short circuit current ($I_{SC}$), open circuit voltage ($V_{OC}$), fill factor ($FF$) and conversion efficiency of a $W_{SC} = 0.2 \mu m$ solar cell are calculated for cases when there is: (a) no GB (hence the material is single-crystalline (sC)), (b) one GB placed $W_{SC}/4$ distance away from the n+ region (1GB) and (c) when there are two GBs, each placed $W_{SC}/4$ distance away from the n+ and p+ regions,

![Fig. 2](image)

Fig. 2 The top view of (a) the proposed solar cell and (b) the cross-section of the simulated device.

### TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_{D+},N_{A},N_{A+}$</td>
<td>$10^{18}, 10^{15}, 10^{18} \text{ cm}^{-3}$</td>
</tr>
<tr>
<td>$W_{SC}$</td>
<td>0.2 - 0.8 μm</td>
</tr>
<tr>
<td>$W_{CON}$</td>
<td>50 nm</td>
</tr>
<tr>
<td>$t_{Si}$</td>
<td>0.2 - 0.8 μm</td>
</tr>
<tr>
<td>$t_{SiN4}$, $t_{SiO2}$</td>
<td>46 nm, 50 nm</td>
</tr>
</tbody>
</table>

Doping concentrations for n+, p, p+ regions ($N_{D+}, N_A, N_{A+}$), width of p region ($W_{SC}$), width of contact region ($W_{CON}$); Si, Si$_3$N$_4$, SiO$_2$ thicknesses ($t_{Si}, t_{SiN4}, t_{SiO2}$).

![Fig. 3](image)

Fig. 3 2D Sentaurus results (●) vs 1D simulation results when there is (a) no GB (●), (b) there is one GB with $N_T = 10^{15} \text{ cm}^{-3}$ (○), (c) there are two GBs with $N_T = 10^{16} \text{ cm}^{-3}$ (+), (d) there is one GB with $N_T = 5x10^{15} \text{ cm}^{-3}$ (●), (e) there are two GBs with $N_T = 5x10^{16} \text{ cm}^{-3}$ (●) within a single device.

![Fig. 4](image)

Fig. 4 Efficiency values of 1 cm$^2$ solar cells simulated for processes with different average grain sizes (GrSs) and GB trap densities ($N_T$s).
respectively \((2GB)\). As shown in Fig. 3, although there are slight mismatches due to 2D effects, results of the proposed model match well with Sentaurus results overall. Another observation from Fig. 3 is the rapid reduction in efficiency with the presence of a single \(GB\) even though the \(N_T\) is low. On the other hand, introducing a second \(GB\) does not reduce the efficiency dramatically.

Once the proposed 1D micro-scale solar cell model is calibrated, the performance of a 1 cm\(^2\) solar cell is simulated. For this purpose, 100 unit cells with \(W_SC = 0.2 \mu m\) and random number of \(GBs\) at random locations are simulated. Afterwards, their SPICE models are connected in parallel to make up a 1 cm\(^2\) solar cell. The \(GBs\) in these devices are placed based on the lognormal distribution with average \(GrSs\) of 0.2, 0.5 and 1\(\mu m\) and a standard deviation of 0.4 \(\mu m\). The contact sheet resistances between these unit cells are neglected and the results are plotted in Fig. 4. Here, it can be observed that the efficiencies of 1 cm\(^2\) cells for \(GrS = 0.2 \mu m\) and \(N_T = 5 \times 10^{18} \text{ cm}^{-3}\) are similar to the efficiencies of poly cells (1\(GB\) or 2\(GB\)) with the same \(N_T\) in Fig. 3. The efficiency of a 1 cm\(^2\) cell improves with the \(GrS\), especially for thicker samples. Yet, the efficiency values remain lower than the \(sC\) results in Fig. 3. This trend occurs due to the unit cells with one or more \(GBs\) which sink the current in an exponential fashion. These defective unit cells dominate the 1 cm\(^2\) cell’s efficiency even though the probability of having a \(GB\) within a unit cell decreases significantly for larger \(GrSs\).

### III. Thin Film Transistor Modeling

To realize a polysilicon based wireless sensor node, the transistors are modeled with the same process used for the energy source. The authors previously proposed a narrow channel polysilicon \(TFT\) for digital [11] and analog [14] applications. Aiming for good performance in both applications, the 2D \(TFT\) model in Fig. 5 is designed with the parameters in Table II in Sentaurus. Similar to the solar cell, the \(GBs\) in the \(TFTs\) are assumed to be unidirectional and perpendicular to the current flow. They also have the same \(N_T\)s and trap energy levels. The gate oxide thickness is determined such that the p-type \(TFT\) (\(pTFT\)) could be operated at the supply voltage required by the sensing and communication units. Since the energy harvesting unit is targeted to power a sensing unit similar to the commercially available TELEOS wireless sensing node [15], the supply voltage is chosen to be 2.4 V and oxide thickness is scaled down to 15 nm.

With the model in hand, the variation in threshold voltage \(V_{TH}\) due to the number and \(N_T\) of \(GBs\) are studied. To do that, \(GBs\) are placed randomly based on the lognormal distributions used for solar cells and 100 \(TFT\) samples with a channel length \((L_{CH})\) of 0.5 \(\mu m\) are simulated. Due to the Aluminum metal work function of the gate, the \(V_{TH}\) of \(pTFT\) is found to be much higher than that of \(nTFT\).

![Cross-section of the simulated nTFT](image)

**TABLE II**

<table>
<thead>
<tr>
<th>TFT Device Parameters</th>
</tr>
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<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>(L_{CH})</td>
</tr>
<tr>
<td>(t_{Si, SiO2})</td>
</tr>
<tr>
<td>(N_{S}, N_{D})</td>
</tr>
<tr>
<td>(N_{Dbody})</td>
</tr>
<tr>
<td>(N_{Abody})</td>
</tr>
</tbody>
</table>

Channel Length \((L_{CH})\), Si and SiO\(_2\) thicknesses \((t_{Si}, t_{SiO2})\), doping concentrations for source and drain regions \((N_{S}, N_{D})\), \(pTFT\) Body Doping \((N_{Dbody})\), \(nTFT\) Body Doping \((N_{Abody})\).

**TABLE III**

<table>
<thead>
<tr>
<th>(sC)</th>
<th>(N_T = 10^{18} \text{ cm}^{-3})</th>
<th>(N_T = 5 \times 10^{18} \text{ cm}^{-3})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(nTFT)</td>
<td>0.14 V</td>
<td>0.22 V</td>
</tr>
<tr>
<td>(pTFT)</td>
<td>0.75 V</td>
<td>0.87 V</td>
</tr>
</tbody>
</table>

![Threshold voltage distributions of pTFTs simulated for the processes with \(N_T = 5 \times 10^{18} \text{ cm}^{-3}\) and average grain sizes (GrSs) of 0.2, 0.5 and 1 \(\mu m\)](image)
It is clear from Fig. 6 that if GrS of the process is comparable to \(L_{CH}\) (as in Fig. 6b), the TFTs might be \(sc\) and \(V_{TH}\) of the devices is far smaller than its \(poly\) counterparts. As the \(GrS\) is increased (from Fig. 6a to Fig 6c), the variation in \(V_{TH}\) values gets larger. For the process in Fig. 6b, the difference in \(V_{TH}\) values is found to be ~ 0.7V and 4 significant peaks are observed. These peaks indicate 4 different distributions for cases when: (a) the device is \(sc\), (b) there is 1 GB where the GB occurs at a non-critical position (close to the drain region), (c) there is 1 GB occurring at a critical position (close to the source region) and (d) there are two or more GBs occurring in the device. This wide variation can be avoided by increasing the \(GrS\) (e.g. to 1 \(\mu m\)) so that the probability of having \(sc\) case is more likely as shown in Fig. 6c.

To do circuit simulations, two SPICE models are created: one for the \(sc\) TFTs (case a (explained above)) and another for the \(poly\) TFTs (cases b, c and d) using the level 62 RPI TFT model [16]. For the \(poly\) case, a representative device is chosen by making a boxplot of the simulated \(V_{TH}\) values and picking the device with mean \(V_{TH}\) value. The \(poly\) SPICE model is designed for the process with \(GrS = 0.2 \mu m\). The model is kept the same across different \(GrSs\), since the mean \(V_{TH}\) does not change significantly with respect to \(GrS\) (maximum deviation from the mean \(V_{TH}\) of the \(GrS = 0.2 \mu m\) case is found to be 8%). Obtained \(V_{TH}\)s are reported in Table III, which indicates that the circuit as well as the system performance will be limited by the performance of the \(pTFT\).

IV. POWER CONVERTER DESIGN

As previously stated in Section III, the system supply voltage requirement for the wireless sensor node under consideration is 2.4 V. Given that the \(V_{OC}\) of a single-junction solar cell is less than 0.5 V (as in Fig. 3), the output voltage of the solar cell needs to be converted to 2.4 V. Without loss of generality, the charge pump topology in Fig. 7 is used for this purpose. In this topology, switching capacitance \(C_{SW}\) is charged via \(S1\) and \(S2\) switches during \(\varphi\) phase of the clock. On the other hand, during the \(\bar{\varphi}\) phase, \(C_{SW}\) is charged from the reverse direction by \(S3\) and \(S4\), leading to a voltage increase on both nodes of the capacitance. Again during \(\bar{\varphi}\), the charge stored in \(C_{SW}\) is transferred to the next stage. For the single-stage charge pump in Fig. 7, this charge is transferred to the load capacitance \(C_l\).

Assuming ideal switches and capacitors, one can calculate the output current transferred to the load to be [17]:

\[
I_{OUT} = \frac{I_{SW}C_{SW}}{N} [(N+1)V_{IN} - V_{OUT}] \tag{1}
\]

where \(f_{SW}\) is the clock frequency controlling the switches, \(N\) is the number of power converter stages, \(V_{IN}\) is the source voltage and \(V_{OUT}\) is the voltage at the output. \(I_{OUT}\) is determined by the equivalent resistance of switching capacitance \((R_{SW})\). Note that, \(I_{OUT}\) is linearly proportional to \(f_{SW}\) as shown in Fig. 8. On the other hand, unlike ideal switches, TFT switches have finite on resistances \((R_{ONs})\) which become comparable to \(R_{SW}\) at high frequencies. This change in dominant resistive element causes the plateau observed for \(I_{OUT}\) at high frequencies (see Fig. 8) which is described as the fast switching limit in literature [18]. In this study, the frequency for which \(I_{OUT}\) deviates from the ideal switch behavior by 10% is defined as the knee frequency \((f_k)\).

For the switches modeled with the TFT model with \(N_T = 5 \times 10^{18} \text{ cm}^{-3}\) (high \(N_T\)) and \(L_{CH} = 0.5 \text{ mm}, f_k\) occurs at 1 MHz. To reduce \(R_{ON}, \text{ TFT width (W_{TFT})}\) can be increased (e.g. to 5 mm) with a corresponding increase in \(f_k\) (to 4.6 MHz). Yet, as the switches get larger so do the gate capacitances of TFTs and the switching loss due to charging and discharging of these capacitances. In addition to the switching loss, the circuit would be more prone to clock feedthrough problem [19]. Therefore, there is a limit to the improvement in \(f_k\) that can be obtained by increasing \(W_{TFT}\). Another way of improving \(f_k\) would be to reduce \(N_T\) (e.g. to \(10^{18} \text{ cm}^{-3}\)), leading to an \(f_k\) of 8.9 MHz, which is very similar to the \(sc\) case with an \(f_k\) of 9.6 MHz.

V. ENERGY SCAVENGING SYSTEM DESIGN

A. System Optimization

To study the effects of process conditions on wireless sensor nodes, the building blocks modeled in the previous sections are put together as shown in Fig. 9. The solar cell as the energy source is represented with its SPICE model. Note, the series and the shunt resistances are not taken into account due to the small size of the cell. The solar cell output voltage is provided at the input of the single-stage power converter.
and converted to 2.4 V \( (V_{OUT}) \). By selecting lower number of stages for the power converter, the number of switches and the switching loss are minimized. The harvested energy is stored in \( C_i \) which acts as the energy buffer. An inverter chain is designed to drive the gates of the \( TFT \) switches in the power converter and estimate the switching loss. Previously, the control unit that regulates the \( f_{SW} \) and the input resistance of the power converter was implemented with a voltage controlled oscillator \( (VCO) \) and a driver [20]. Since the power consumption of the \( VCO \) was negligible with respect to the switching loss, it is omitted in this analysis. Therefore, the initial clock signal \( (\varphi) \) is provided by an ideal voltage source. In addition to that, the supply voltage of the gate driver is provided by the energy buffer. Thus, the net system \( I_{OUT} \) is obtained to be less than what is harvested from the solar cell.

To optimize the performance of the system in Fig. 9, the design flow in Fig. 10 is employed. Before starting the design, the power and area requirements for the system are determined. The system is investigated for the three processes whose parameters are shown in Table IV. From these parameters, \( N_T \) and \( GrS \) are common for both solar cell and \( TFTs \) while \( t_Si \) and \( W_{SC} \) are solar cell specific. The results for these three processes are compared to demonstrate the change in system performance with respect to process conditions.

### TABLE IV

<table>
<thead>
<tr>
<th>Process Parameters Considered in the System Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N_T ) (cm(^{-3}))</td>
</tr>
<tr>
<td>--------------------------</td>
</tr>
<tr>
<td>Worst</td>
</tr>
<tr>
<td>Average</td>
</tr>
<tr>
<td>Best</td>
</tr>
</tbody>
</table>

The design process is initiated with determining the maximum \( V_{TH} \) required by the power converter. Based on this criterion, the \( TFT \) is designed with the model explained in Section III, whereas the solar cell is modeled as in Section II. Afterwards, the 1 cm\(^2\) solar cell is divided into \( M \) regions that are connected in series. Finally, to optimize the system performance, system output power \( (P_{OUT}) \) is monitored for different solar cell array configurations. For each configuration, the \( W_{TFT} \) is optimized while the gate driver is scaled accordingly. Note that, this framework gives the user multiple options to improve the system performance. One can improve solar cell process parameters, redesign \( TFT \) for a better performance or optimize number of power converter stages to improve the \( P_{OUT} \) if system requirements are not met.

The results for the \( W_{TFT} \) optimization for the “Worst” process with \( M = 7 \) is shown in Fig. 11. The results indicate an optimum \( W_{TFT} \) for the best system performance. For a small \( W_{TFT} \) (e.g. 1.4 mm) \( R_{ON} \) of the transistor is high and the transistor cannot provide the required current at that range of frequency. On the other hand, for large \( W_{TFT} \), e.g. 2 mm, the switching loss at the gate driver manifests itself at higher frequencies since it is linearly proportional to \( f_{SW} \) \( (P_{SW} = CV_{DD}^2) \). The optimum \( W_{TFT} \) is observed to be 1.8 mm, with the system operating at 1.75 MHz to provide the best performance.

This study is extended for different processes and different \( Ms \). The maximum net \( I_{OUTS} \) for each \( M \) \( (M_{MAX}) \) are reported in Fig. 12. The results show that the optimum \( Ms \) for the cells fabricated with the ‘Best’, ‘Average’ and the ‘Worst’ case processes in the design space are 4, 6, and 7 respectively. For \( Ms \) smaller than the optimum ones, the maximum current that the solar cell can provide is high. Hence, the power converter

---

Fig. 9 Energy scavenging system schematic

Fig. 10 Bottom-up design flow for the micro-scale energy harvesting system in Fig. 9.
needs to operate at high frequencies with higher switching loss. Besides, the converter might be operating close to or beyond its $f_x$ which would again limit $I_{OUT}$. Therefore, $I_{OUT}$ obtained at a lower frequency would provide better results. In such a case, the maximum operating point of the solar cell when it is isolated from the system ($V_{MAX}$, $I_{MAX}$) is different than its optimum operating point when it is connected to the system ($V_{SYS}$, $I_{SYS}$). For $M$s higher than the optimum value, $I_{MAX}$ scales down while $V_{MAX}$ increases. However, due to lower overdrive voltages for $nTFT$ and asymmetric performance of $nTFT$ and $pTFT$, the input resistance of the power converter also increases with $V_{IN}$. Hence, the system $I_{OUT}$ reduces.

Finally, the power conversion efficiency is also found to be changing with process parameters. For the “Best” process with $M = 4$, the power conversion efficiency of the converter is found to be 89% while it is observed to be 86% and 78% for the “Average” process with $M = 6$ and the “Worst” process with $M = 7$.

**B. Effect of Process on the System Performance**

When the maximum $I_{MAX}$ values for the “Best”, “Average” and “Worst” cases in Fig. 12 are compared, a significant change can be observed. This change roots both from the change in the solar cell and $TFT$ performance with the changes in the process. In this subsection, the contribution of each device is quantified and how the process parameters change the overall system performance is studied.

1) **Effects of $GrS$ on the System Performance**

For the “Worst” process, if $GrS$ of the process increases from 0.2 µm to 1 µm, the probability of having no $GB$ in the device increases significantly (see Fig. 6). Provided $GrS$ is fixed for the solar cell model, the improvement in the system performance would be solely due to the improvement in $TFT$ and the power converter performance. To study this improvement, the system is designed both with $sC$ and $poly$ $TFT$s driven by ideal clocks ($Clk_{ideal}$ case). The results in Fig. 13 indicate that the output current can increase slightly (by 20 µA) if the $TFT$ model is switched from the $poly$ model with high $N_T$ to $sC$ one. In the next stage, the switching power loss is taken into account by implementing gate drivers ($Clk_{GD}$) or by ideal voltage sources ($Clk_{ideal}$).

2) **Effects of $N_T$ on the System Performance**

As a second case study, the fabrication process is changed from the “Average” to the “Best” cases in Table IV. Fig. 14 System performance improvement when the fabrication process is changed from “Average” to the “Best” cases in Table IV.
to the green square curve and the improvement would reduce to 355 µW. On the other hand, when the system is actually fabricated, the “Best” cell would be interfaced with a power converter employing the low NF TFT model (see Table IV). Therefore, the system’s actual IOUT is the blue diamond curve in Fig. 14. Once the TFT model is changed, the output power of the system fabricated with the “Best” solar cell improves by 867 µW. Hence, the system output power improves by 1222 µW when the process is changed from the “Average” to the “Best”. These results indicate that the solar cell output power can increase significantly. Yet, the net harvested power is going to be limited by the TFT performance.

VI. CONCLUSION

In this paper, a bottom-up modeling approach is applied to study the performance of an integrated LTPS micro-scale energy harvesting system. At device level, solar cell performance is found to reduce sharply with introduction of NF unlike TFTs. On the other hand, a significant variation in TFT performance is observed for small L crit, which can be kept under control by obtaining larger Gr S. At the circuit level, the operation frequencies (and therefore the maximum IOUT) of the power converters employing TFTs are demonstrated to be limited by their RON. At the system level, the optimum operating point of a solar cell is found to change when it is connected to the power conversion system. Due to the losses in the power conversion circuitry, net IOUT can be increased by reducing fsw and the switching loss. In addition, the system performance is found to be heavily affected by the process parameters. For instance, the area of the circuit can be reduced 20 times if the Grs of the TFT’s are increased for the “Worst” process in Table IV. On the other hand, it is shown that even though the performance of the solar cell is improved by changing process parameters, the TFT performance can still significantly limit the system performance. Finally, it is demonstrated that high power conversion efficiencies (78 to 89%) can be achieved by using poly TFTs.

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