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ABSTRACT This paper presents the simulation model, performance evaluation and hardware implementation of a technique to resolve phase ambiguity in trellis coded modulation (TCM) where the popular Viterbi algorithm is utilized. While this approach has been employed with BPSK and QPSK, its application to multilevel modulation schemes (M>4) is novel and of interest because it provides a viable alternative to rotationally invariant codes. This approach does not require any arithmetic computations and can be accomplished with minimal hardware. The results presented in this paper are being used to implement a 32 sector phase quantized TCM system utilizing 8PSK modulation*.

I. INTRODUCTION

Development of spectrally efficient communication systems is of interest due to increasing spectral congestion. Future communication systems must not only be spectrally efficient, but also operate at high data rates with low error probabilities under stringent power constraints. These features become essential for space communications where extensive video transmission is desired.

Since constant envelope modulation techniques such as phase shift keying (PSK) are less susceptible to intermodulation interference and other anomalies induced by traveling-wave tube amplifiers, they are more suitable for space communication. Today, a majority of communication links employ either BPSK or QPSK. The need to transmit greater quantities of data through bandlimited channels has spurred research and development of communication systems which utilize higher level modulation (M>4).

Trellis coded modulation (TCM) [1,2] is a method of combining convolutional coding and multilevel modulation techniques such as PSK and QAM to provide spectrally efficient communication. While there has been considerable research in this area over the past ten years there are still a number of implementation questions that need to be addressed.

One problem which adds to hardware complexity and requires special attention arises due to the indiscriminate nature of the phase detection process in the carrier tracking loop. Phase ambiguities exist because the transmitted signal elements and the demodulated signal elements at the receiver can have a $2\pi/M$ phase rotation for M-PSK (M=2,4,8,...).

Figure 1 is the block diagram for a TCM receiver. The input, r(t), is modeled as $r(t) = A\cos(\omega_c t+\phi_i)+w(t)$, $0<t<T_s$, where $\phi_i = 2(i-1)\pi/M$ $(i=1,2,3,\ldots,M)$ represents one of M possible transmitted messages and w(t) is the additive wideband Gaussian noise. The demodulator output, $\hat{\phi}_n$, is a quantized version of the received phase constellation [3,4,5].

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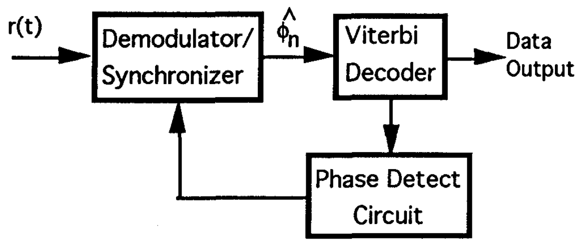

Figure1. Block Diagram of a TCM Receiver

There are two methods to deal with phase ambiguities. One approach constrains the design of the TCM code to those which are rotationally invariant [6,7]. These codes sacrifice performance for the ability to correctly decode at any $2\pi/M$ phase rotations between the transmitted and the received signal elements. In addition, rotationally invariant codes (excluding 180°) tend to increase implementation complexity. The second approach is to detect the condition of being out of phase and adjust the demodulator to resolve the problem [8]. In this paper we present a simple phase detection model, provide a performance evaluation and examine its implementation complexity.

Since 180° rotationally invariant codes can be constructed from non-rotationally invariant codes without sacrificing coding gain or increasing complexity, they are distinct from codes that are 45° and 90° rotationally invariant [6]. The advantages mentioned above make detection and correction an alternative to rotationally invariant codes.

II. PHASE DETECTION MODEL

The general approach taken to design the phase detection portion of the decoder was to examine the decoders cumulative path metrics under various conditions to determine their usefulness in detecting the out-of-phase conditions. A mathematical description of the branch metrics and the cumulative metrics is available from [9,10].

The proposed phase state detection scheme is based on the fact that the cumulative metrics grow at a faster rate if the decoder is processing data based on an incorrect phase state, than they will if the decoder is receiving data from a correct phase state. Since the metrics reflect the amount of certainty in the data, during an out-of-phase condition the error rate is large ($\approx 1/2$) and the cumulative metrics grow at a faster rate. When the in-phase condition exists the branch metrics represent less uncertainty in the data and take on smaller numbers, thus, the cumulative metrics grow at a relatively slower rate.

One of the most appealing aspects of this detection scheme is that there are no arithmetic computations necessary to implement this model. This is because the observed variable is a binary scaled version of a cumulative metric already available within the VA. Utilizing the m_{th} least significant bit (LSB) of a cumulative metric as a test bit results in a divide by 2^m count of the cumulative metric. The test bit, the m_{th} LSB, should be chosen such that $2^m \geq B$, where B is the maximum branch metric. The test bit can be used to drive a counter and at the end of N symbols the counters output, the test word, can be compared to the threshold and a decision rendered. A block diagram is shown in Figure 2.

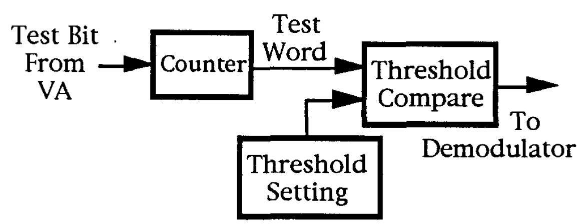

Figure 2. Block Diagram of the PDC

Because the minimum length path can change from one node in the trellis at time k to a different node at time k+1, the statistics of all the cumulative metrics are identical. This means the test bit can be selected from any one of the cumulative metrics in the manner prescribed above. In addition, other than the phase condition and signal-to-noise ratio (SNR), the value of the test word depends only on the maximum assigned branch metric, B, and the window size N. Thus, this technique will work with any Viterbi decoder.

Simulations were performed which included transmitter and receiver signal constellation phase rotations of 45°, 90° and 135°. It was observed that the metric growth rate could be modeled as a Gaussian random variable with mean μ and standard deviation σ. Phase rotations of 45° and 135° yielded $\mu = 51.89$ and $\sigma = 1.10$ which correspond to the worst case, while the in-phase simulation results yielded $\mu = 36.41$ and $\sigma = 1.87$.

Histograms from the simulation results are shown in Figure 3 superimposed on the observed variable, Z, modeled as a Gaussian random variable with the means and standard deviations specified above. Simulations ran with N=256, B=15 and 1.020e8 symbols which corresponds to 400,000 samples of Z. The SNR was $E_b/N_0 = 5.5$ dB corresponding to BER = 2.0e-3.

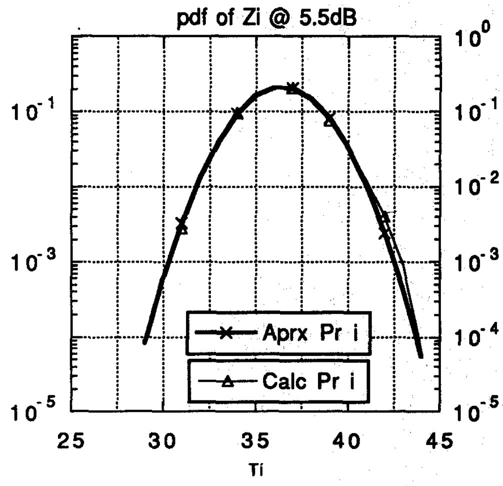

Figure 3A. In-Phase Simulation vs Gaussian Approximation.

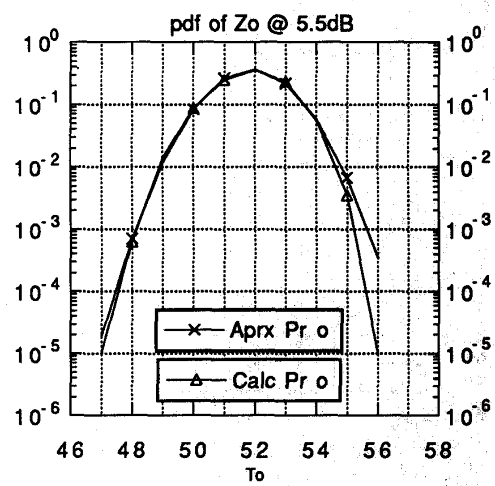

Figure 3B. Out-of-Phase Simulation vs Gaussian Approximation

Two conditional probabilities, P_a and P_b, were used to characterize the performance of the phase detect circuit (PDC). Under the correct phase $P_a = P[Z \geq \mu + z\sigma/\phi]$ and under the incorrect phase $P_b = P[Z \leq \mu - z\sigma/\phi]$. Thus, P_a is the probability the PDC will incorrectly interrupt a good data stream and declare an out-of-phase condition exists and P_b is the probability the PDC will incorrectly declare a bad data stream valid during an out-of-phase condition. Rewriting these probabilities in terms of the function Q[k], where

$$Q[k] = \frac{1}{\sqrt{2\pi)}} \int_{k}^{\infty} e^{-\lambda^2/2}\, d\lambda$$

yields $P_a=Q[(\mu_i-z)/\sigma_i]$ and $P_b=Q[(z-\mu_o)/\sigma_o]$ where 'i' denotes in-phase, 'o' denotes out-of-phase and Z is the threshold. Figure 4 illustrates the behavior of P_a and P_b as a function of the threshold using the Gaussian model as well as direct simulation results. The critical BER in many applications is approximately 10^{-3}, therefore performance of the PDC for BER $< 10^{-3}$ was not considered.

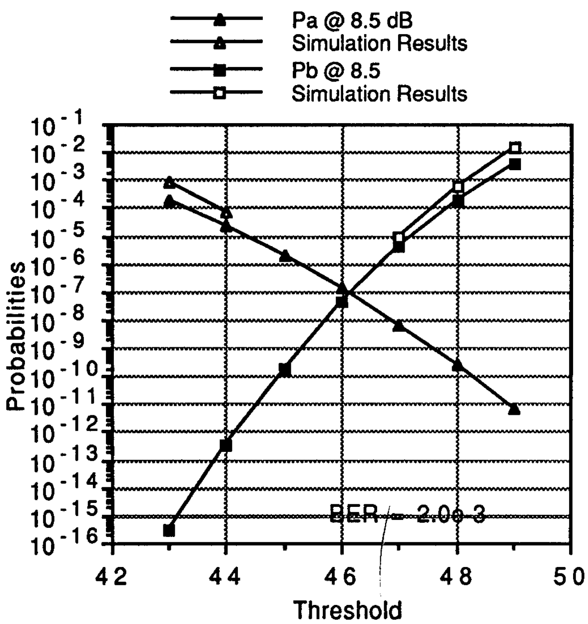

Figure 4. Tradeoff Characteristics

III. PERFORMANCE ANALYSIS

Evaluation of the PDC's performance was done by determining two figures of merit. We first considered the impact of a wrong decision on the overall system BER (BER_{sys}), and secondly, we determined the mean time to acquire (MTA). The result bounded P_a and an optimum operating threshold was determine.

To analyze the impact an incorrect decision has on BER_{sys}, we considered the ensuing events. A critical error occurs when steady state operation is interrupted by an incorrect decision. Since 180° phase invariance exists, a minimum of 4 rotations (each $\pi/4$) are required to regain phase lock. An event starts when phase lock is lost and ends when correct phase lock is regained. The probability of making i consecutive incorrect decisions within this event, which means an additional (2N)(i+1) bits of data will be effected, can be written as

$$P[i] = P_a P_b{}^i (1 - P_b)^3$$

where i=0,1,2,3,... and P_a and P_b are defined above. We realistically assumed P_b<<1 and therefore neglected consecutive incorrect decisions within the event. The number of incorrect bits in this event is (4)(2N) and the bit errors resulting from a false decision (BER_{fd}) is given by

$$BER_{fd} \approx (4)(2N)P[0] = (8N)(P_a) \quad (1)$$

To ensure that BER_{fd} would not significantly impact the system BER we required that BER_{fd} be at least one order of magnitude less then BER_{sys}. At $BER_{sys}=10^{-3}$ and N=256, Equation 1 resulted in the inequality

$$P_a \leq 4.9e\text{-}8.$$

We followed a similar analysis to determine the MTA. The worst case occurs when the demodulator locks on a phase just past the correct phase and a minimum of three phase adjustments are required to gain proper lock. The probability of making i consecutive incorrect decisions becomes

$$P[i] = P_b^{\,i} (1 - P_b)^3$$

where i = 0,1,2,... and the number of bits for this event becomes (3)(2N)(i+1). Again, assuming P_b<<1 the expression for MTA becomes

$$MTA \leq 6N \quad \text{bits.}$$

III. IMPLEMENTATION AND DISCUSSION

The most appealing aspect of this technique is that it requires remarkably little hardware to implement. The processor implementation requires only one 8 bit counter and one 8 bit comparator. The test bit from the cumulative metric triggers the counter to generate the test word. The test word is compared to the threshold setting and a decision is rendered. The control circuit consists of one 8 bit counter triggered by the symbol clock and an AND gate which resets the circuit every N symbols.

To get an idea of the PDC's performance, consider a bit rate of 100 Mb/s, N = 256 symbols and a single threshold setting of 47. We would like to determine how long phase acquisition takes and the mean time between false alarms. The MTA is at most 3N or 768 symbols. At a BER of only 2.0e-3, $P_a = 10^{-8}$ and $P_b = 10^{-5}$, the mean time between false alarms will be 1 sec. In contrast, at a reasonable BER of 10^{-5} (P_a = 6.4e-32, P_b = 6.9e-4) the mean time between false alarms is 2.0e25 years.

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