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A Fully Programmable Analog Window Comparator

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***Abstract*— This paper presents a novel design of analog window comparator circuit. The comparator can adaptively adjust its error threshold according to the magnitude of input signal levels. In addition, the circuit can be digitally programmed to realize different error threshold adapting schemes. The design is fabricated using a 0.18μ CMOS technology. Testing results of the fabricated chip are also presented.**

I. INTRODUCTION

Analog window comparators are widely used in analog testing applications [1], [2], [3]. Such circuits monitor the difference between signals under scrutiny and report circuit malfunctions when signal difference exceeds its normal range. An analog window comparator usually contains two analog inputs and a digital output. Its output switches from one logic value to the other when the difference between window comparator inputs exceeds the range of $[-V_\epsilon, V_\epsilon]$, where V_ϵ is referred to as the window comparator error threshold.

There are three types of window comparator error thresholds, namely *constant*, *relative*, and *adaptive* error thresholds. In the first category [4], [5], [6], [7], [8], [9], [10], [11], [12], the error threshold of a window comparator is constant regardless of its input signal levels. This type of window comparators quickly lose their fault-detection capabilities when signals being monitored become small. While window comparators with relative error thresholds [8], [13] overcome such problems by making their error thresholds proportional to input signal levels, the drawback associated with the relative error threshold scheme is that error thresholds become too small when window comparator inputs are close to the signal ground level. Thus, small differences caused by tolerable circuit mismatches may be incorrectly identified as faults. Analog checkers with adaptive error thresholds are presented in [13], [14], [15]. They use a pair of inverters to digitize the amplified input difference. The adaptive error threshold is implemented by dynamically adjusting the impedance of the pull-up paths of the two inverters according to input signal levels. Improved concurrent error detection capabilities have been reported with using these comparators.

In many analog online testing applications, a single analog window comparator is time-shared to test different parts of the circuit [1], [16], [17]. To achieve high fault detection capabilities, the error threshold of the comparator is preferred to be attuned to the characteristics of the sub circuit under test. Most of the previously proposed window comparators do not provide the flexibility to program the error threshold after the circuit design is complete. Although a mechanism to vary the comparator threshold is presented in [1], the technique is applicable to the constant error threshold scheme only. In this paper we present a fully programmable window comparator with adaptive error threshold.

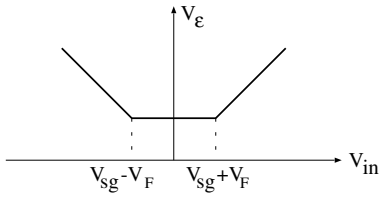

Fig. 1. Adaptive threshold

The implemented adaptive error threshold is shown in Figure 1. When its input signals are large, the proposed window comparator uses the relative error threshold scheme. If the window comparator experiences small input signals, it switches to the constant error threshold method. By adaptively selecting error thresholds, the proposed window comparator will efficiently detect circuit faults no matter input signals being large or small.

For the convenience of discussion, we assume input signals are centered at the signal ground level V_{sg} and the maximum peak-to-peak value of the input is $2 \cdot V_A$. We refer to the region that the comparator has a constant error threshold as the *flat band region*. The voltage, V_F, at which the window comparator switches from the constant error threshold mode to the relative error threshold mode, is called *flat band voltage*. The ratio of V_F to V_A is called *flat band ratio* and denoted by symbol $\mathcal{R}$. In addition, the comparator error threshold in the constant threshold region is defined as the minimum error threshold V_ϵ^{min}. The slope of the error threshold curve in the relative error threshold region is called threshold gain g_ϵ. An appealing feature of the proposed design is that parameters $\mathcal{R}$, V_ϵ^{min}, and g_ϵ, which characterize the comparator threshold adapting schemes, can be digitally programmed. This flexibility makes the proposed circuit extremely desirable in various analog online testing applications.

The rest of the paper is organized as follows. Section 2 describes the proposed design. Section 3 presents experimental results and the paper is concluded in Section 4.

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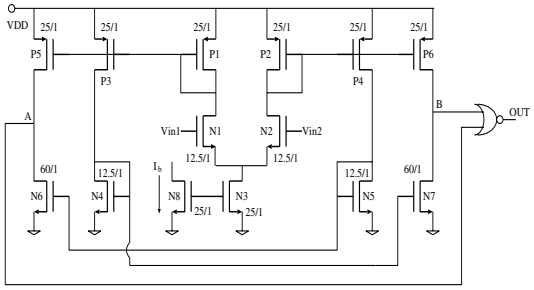

Fig. 2. Proposed checker circuit

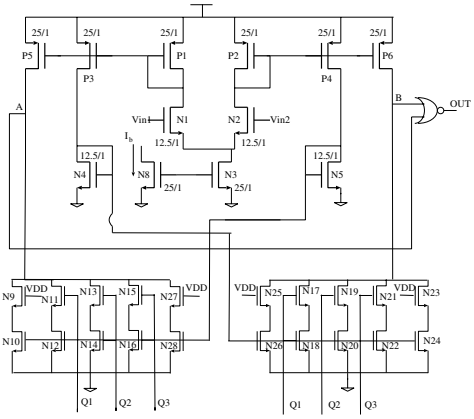

Fig. 3. Modified checker circuit

II. Circuit description

The proposed design consists of an adaptive biasing circuit and a checker circuit whose error threshold can be programmed through its biasing current.

A. Checker circuit

The checker circuit, as shown in Figure 2, is comprised of a differential input pair and four current mirrors. Transistors N_1 and N_2 constitute the differential pair. PMOS devices $P_1 \sim P_6$, which have the same size, implement two sets of PMOS current mirrors. Transistors N_4 and N_7, N_5 and N_6, realize two NMOS current mirrors with a current gain of m (the size of N_6 and N_7 is m times larger than that of N_4 and N_5). Assume the current flowing through N_3 is I_b. When both checker inputs are at the same level, N_1, N_2, N_4, N_5, and $P_1 \sim P6$ are in their saturation regions; and all the currents flowing through these transistors are $\frac{I_b}{2}$. N_6 and N_7, working in their linear regions, pull voltages at nodes A and B close to ground, driving the checker output to logic *1*.

Without losing generalities, assume checker input V_{in1} becomes larger than input V_{in2}. Consequently, currents flowing through N_1 and N_2 become $\frac{I_b}{2} + i$ and $\frac{I_b}{2} - i$, where i is the current variation caused by the difference between checker inputs. When $\frac{I_b}{2} + i > m \cdot (\frac{I_b}{2} - i)$, the voltage at node A is pushed close to V_{DD} and, hence, the checker output switches to logic *0*.

Assuming that I_{DS} and V_{GS} relations of N_1 and N_2 follow the perfect square-law, the checker error threshold can be derived as:

$$V_\epsilon = \sqrt{\frac{2 \cdot I_b}{\mu_n \cdot C_{ox} \cdot (W/L)_{N1,2}}} \cdot \sqrt{1 - \sqrt{1 - (\frac{m-1}{m+1})^2}} \quad (1)$$

where μ_n is the carrier mobility; C_{ox} is the transistor gate unit capacitance; and $(W/L)_{N1,2}$ is the size of N_1 and N_2.

The above equation shows that the comparator threshold can be adjusted by varying the value of m. A modified comparator circuit with programmable m values is shown in Figure 3. In the modified design, programmable current mirror (PCM) circuits replace the simple current mirrors ($N_4 \sim N_7$) used in the original design. The output branch of a PCM circuit consists of five current sink paths. Three of them can be turned on or off depending on digital signals Q_1,Q_2,Q_3, which represent a 3-bit thermometer code. The other two paths are always on to keep the minimum value of m as 2. A binary to thermometer code encoder converts two digital programming inputs to thermometer code Q_1,Q_2,Q_3. Assume all the transistors in PCM circuits have the same size, *m* can be programmed from 2 to 5. Consequently, the comparator error threshold can be scaled by factors ranging from 0.24 to 0.5.

B. Programming adaptive biasing circuit

Equation (1) also indicates that the checker error threshold is proportional to the square root of its biasing current. To achieve the adaptive error threshold shown in Figure 1, the biasing current should be proportional to the square of the input magnitude when the input is in the relative error threshold region. When the input is in the constant threshold region, the biasing current should be a constant.

The proposed biasing circuit is given in Figure 4. It includes three current generation blocks, labeled as U_1, U_2, and U_3. Transistors M_{16}-M_{30} generate the output biasing current according to the following equation.

$$I_b = \begin{cases} I_{min} & \text{for} \quad V_{sg} - V_f < V_{in} < V_{sg} + V_f \\ w \cdot I_p & \text{for} \quad V_{in} < V_{sg} - V_f \\ w \cdot I_n & \text{for} \quad V_{in} > V_{sg} + V_f \end{cases} \quad (2)$$

where I_p and I_n are output currents of U_1 and U_2 respectively. w is the scaling factor that is controlled by programmable inputs a and b. When checker input V_{in} is within the *flat band region*, $w \cdot I_p$ (or $w \cdot I_n$) are smaller than I_{min}. In this case, transistor M_{15} will drain current to make sure $I_b = I_{min}$. Hence, the checker has a constant error threshold.

If V_{in} is greater than signal ground level V_{sg}, M_8 in U_2 is off and M_1 in U_1 conducts current. After V_{in} leaves the flat band region, $w \cdot I_n$ becomes larger than I_{min}. Subsequently, M_{15} is off and $I_b = w \cdot I_n$. In the design, I_Q is very small and all the transistors in U_1 are in their saturation regions. Thus,

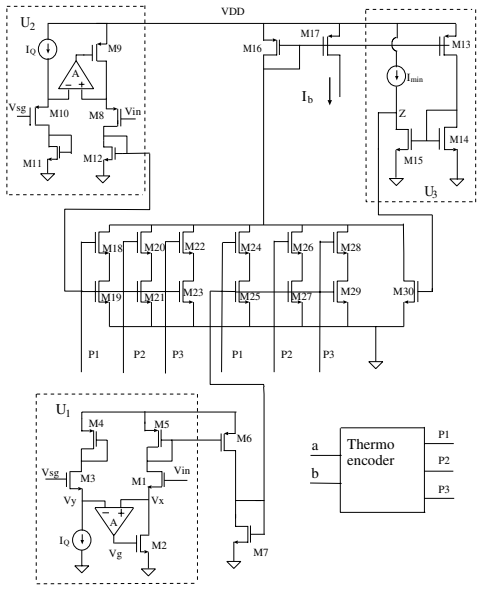

Fig. 4. Proposed adaptive biasing circuit

I_b, which is the same as I_{DS1}, can be derived as:

$$I_b = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{w \cdot (W/L)_{M1}}{1 + \frac{1}{A} \cdot \sqrt{\frac{(W/L)_{M1}}{(W/L)_{M2}}}} \cdot (V_{in} - V_{sg} - \frac{V_t}{A})^2 \quad (3)$$

where V_t is the threshold of MOS devices and A is the gain of the amplifier used in U_1. Ignoring the term of $\frac{V_t}{A}$ in the above equation, the biasing current becomes proportional to the square of the input magnitude ($V_{in} - V_{sg}$). As a result, the checker has relative error thresholds. When V_{in} is smaller than V_{sg} and out of the flat band region, the biasing current I_b, which will be generated by U_2, is also proportional to the square of the input signal magnitude to implement relative error thresholds. Note that the technogy parameters (μ_n and C_{ox}) in comparator threshold equation will be cancelled when substitute I_b into Equation (1). Thus, the comparator threshold becomes independent of technology parameters.

The programmability of the biasing circuit is realized by controlling the scaling factor w. A binary to thermometer code encoder circuit converts 2-bit programming inputs a and b to 3-bit thermometer code P1,P2, P3, which control the status of the current sinking paths in the PCM circuits. When a=0 and b=0, all three programmable current sink paths are off. The biasing current becomes independent of U_1 and U_2 outputs. Thus the comparator circuit has a constant error threshold. Note that varying w values changes both comparator threshold gain and flat band ratio, because a large w value will cause $w \cdot I_n$, or $w \cdot I_p$ exceeds I_{min} early, and resulting a small flat band ratio.

C. Amplifier gain requirement

The selection of amplifier circuits to be used in the biasing circuit is discussed here. If the $\frac{V_t}{A}$ term in Equation 3 is not completely ignored, the expression of I_{DS1} can be re-written as:

$$I_{DS2} \approx \zeta \cdot [(V_{in} - V_{sg})^2 - 2 \cdot (V_{in} - V_{sg}) \cdot \frac{V_t}{A}] \quad (4)$$

where

$$\zeta = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{w \cdot (W/L)_{M1}}{1 + \frac{1}{A} \cdot \sqrt{\frac{(W/L)_{M1}}{(W/L)_{M2}}}} \quad (5)$$

Note that the square term $(\frac{V_t}{A})^2$ is omitted due to its small value. Inside the bracket at the right-hand side of Equation 4, the first term represents the ideal value that will result in a perfect current output; the second term represents a linear error added to the ideal value. Thus, the relative error α[1] of the biasing circuit output can be written as:

$$\alpha \approx \frac{2 \cdot V_t}{A \cdot (V_{in} - V_{sg})} \quad (6)$$

It is easy to see that α has its largest value when the input signal is just beyond the flat band region. Thus, the largest α can be written as:

$$\alpha_{max} = \frac{2 \cdot V_t}{V_A} \cdot \frac{1}{A \cdot \mathcal{R}} \quad (7)$$

We define the relative variation of analog checker error thresholds as:

$$\delta = |\frac{V_\epsilon(ideal) - V_\epsilon(real)}{V_\epsilon(ideal)}| \quad (8)$$

From equation(1)and (7),we find that to achieve a given δ value the minimum amplifier gain requirement is:

$$A_{min} \approx \frac{V_t}{V_A} \cdot \frac{1}{\mathcal{R} \cdot \delta} \quad (9)$$

To validate the above analysis, current simulation are conducted to find the maximum δ values with different amplifier gains and flat band ratios. The findings, plotted in Figure 5, are consistent with our analysis in Equation 9. According to the above discussion, the amplifier gain does not need to be very high. For example, assuming $V_A \approx V_t$, $\mathcal{R} = 1/5$, and $\delta = 10\%$, the required gain is around 50. Therefore, simple single-stage amplifiers can be used in the biasing circuit. In case that a very small δ needs to be achieved, a cascoded circuit topology can be used to boost the amplifier gain. The voltage swing at the amplifier output can be shown to be very small. Thus, it is easy to design cascoded amplifiers for this application even with low power supply.

III. Experiment results

The proposed circuits have been implemented using a 0.18μ CMOS technology. Transistor sizes used in the checker circuit are given in Figure 2. Single-stage differential amplifiers [18] are used in the adaptive biasing circuit. The design requires a single 3.3V power supply and the signal ground level is 1.65V.

Figure 6 shows a testing result of the fabricated chip. The inputs of the checker are two sinusoidal signals with the same magnitude, frequency, and phase. V_{in1} is centered at the signal

[1] $\alpha = \frac{|I_b(ideal) - I_b(real)|}{|I_b(ideal)|}$

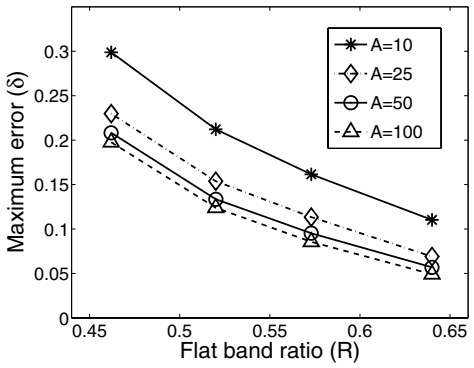

Fig. 5. Effect of amplifier gain on maximum error

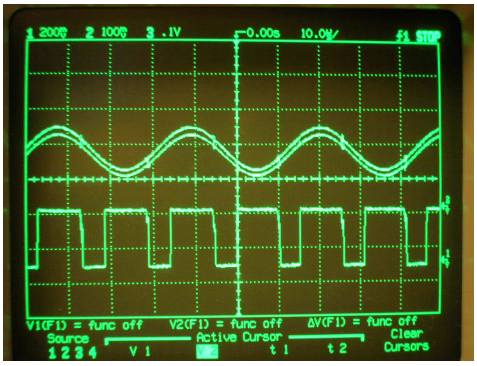

Fig. 6. measurement result of transient inputs

ground level. The offset voltage of V_{in1} is 160 mV higher than that of V_{in2}. Input V_{in1} is also connected to the biasing circuit to control the biasing current. It shows that this difference is detected by the checker (checker output is logic 0) when the signal values are close to the signal ground level. When the inputs are close to their peak values, the same difference is ignored by the checker due to its increased error threshold.

The programmability of the proposed design is also verified by our testing results. Figure 7 shows measured comparator thresholds at different input levels. The four curves in the figure correspond to the realized comparator error thresholds with different digital values applied to the programmable inputs a and b. Note that when both a and b are logic 0, a constant error threshold is realized. With other digital programming input values, the proposed adaptive error threshold scheme is implemented. Also, the threshold gain and flat band ratio vary according to the programmable inputs.

IV. Conclusions

A fully programmable analog window comparator with adaptive error thresholds is developed and testing results of the fabricated chip are presented. Factors affecting the accuracy of the comparator error thresholds are discussed. The proposed window comparator is capable of more effectively detecting circuit faults in analog online testing applications.

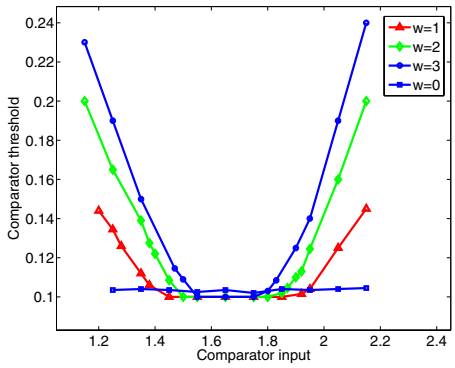

Fig. 7. programmable relative threshold

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