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A Programmable Window Comparator for Analog Online Testing

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Abstract

This paper discusses the challenge of designing window comparators for analog online testing applications. A programmable window comparator with adaptive error threshold is presented. Experimental results demonstrate that improved fault detection capability is achieved by using the proposed design. Measurement results of the fabricated comparator circuit are also presented.

1 Introduction

Online testing has been widely used in mission-critical applications to improve the fidelity of electronic systems. Various techniques have been developed to perform online testing for analog circuits [1, 2, 3, 4, 5, 6, 7]. Among those techniques, an useful approach is to duplicate a portion of the circuit under test and compare the outputs of the original circuit and its replication [1, 8, 9] (redundancy based approach). Analog window comparators are normally used for such purposes. An analog window comparator contains two analog inputs and a digital output. Its output switches from one logic value to the other when the difference between window comparator inputs exceeds the range of $[-V_\epsilon, V_\epsilon]$, where V_ϵ is referred to as the window comparator error threshold.

There are three types of window comparator error thresholds, namely *constant*, *relative*, and *adaptive* error thresholds. In the first category [10, 11, 12, 13, 14, 15, 16, 17, 18], the error threshold of a window comparator is constant regardless of its input signal levels. This type of window comparators quickly lose their fault-detection capabilities when signals being monitored become small. While window comparators with relative error thresholds [14, 19] overcome such problems by making their error thresholds proportional to input signal levels, the drawback associated with such circuits is that error thresholds become too small when window comparator inputs are close to the signal ground level. Thus, small differences caused by tolerable circuit mismatches may be incorrectly identified as faults. Analog checkers with adaptive error thresholds are presented in [19, 20, 21]. These circuits use pairs of inverters to digitize the amplified input difference. The adaptive error threshold is implemented by dynamically adjusting the impedance of the pull-up paths of the inverters according to input signal levels. Improved concurrent error detection capabilities have been reported with using these comparators.

In this paper, we demonstrate the need for programmable adaptive window comparators in online testing analog reconfigurable circuits. We also present a comparator design that can automatically adjust its threshold according to the input signal magnitude. More interestingly, the comparator's error threshold adapting scheme can be digitally programmed. This makes it possible to attune the window comparator for more effectively testing different circuits with distinctive characteristics. Experimental results demonstrate that improved fault detection capability is achieved by using the proposed design. The proposed comparator is fabricated using a 0.18μ CMOS technology. Measurement results of the fabricated comparator are also presented.

The rest of the paper is organized as follows. Section 2 reviews redundancy-based online testing techniques on analog reconfigurable platforms. It also discusses the need for programmable adaptive error threshold and introduces parameters for characterizing the comparator adaptive error threshold. Section 3 describes the proposed comparator design. Experimental results are presented in Section 4, and the paper is concluded in Section 5.

2 Preliminaries

2.1 Analog online testing on reconfigurable hardware platforms.

The redundancy-based online testing scheme is illustrated in Figure 1. In order to reduce testing-hardware overhead, reconfigurable hardware has been used to implement the redundant testing module. By exploiting the reconfigurability, the same hardware can be used to test different sections of the circuit [1, 8, 9, 22].

Recently Field Programmable Analog Arrays (FPAAs) have emerged as a promising platform to implement analog circuits with fault recovery capability [23]. To cost-effectively detect faults occurred in an FPAA circuit, a set

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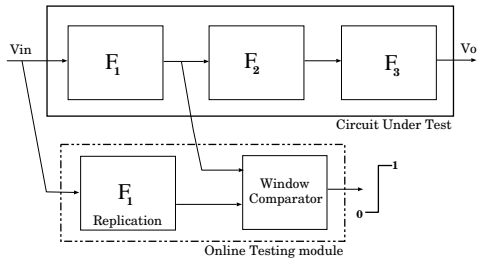

Figure 1. Redundancy based On-line testing.

of configurable resources can be periodically programmed to replicate different sections of the circuit under test (CUT). The output of the original circuit and the replication are monitored by a window comparator to detect the occurrence of faults. By taking advantage of dynamic reconfiguration capability of modern FPAAs, testing operations can be carried out without interrupting the normal operation of the circuit. When a circuit fault is detected, FPAAs can be reconfigured to replace the fault component with unused resources. Since different sections of a circuit may have distinctive characteristics, they may require custom designed comparator error threshold in order to achieve high fault detection capability. This is elaborated in the following section.

2.2 Optimal comparator error threshold

In the testing setup shown in Figure 1, the output of the original circuit and its replication should be identical in the ideal case. However, due to device mismatches and circuit parasitics, normally there is a small difference between the outputs of the two circuits even in the fault free scenario. Consequently, the error threshold of the window comparator should be selected slightly larger than this difference in order to detect faulty circuits and ignore the variations caused by the above circuit non-ideal effects. Assume the CUT is a linear circuit. For given tolerable circuit mismatches, the difference between the original and its replication (here after referred to as ΔV) is proportional to the magnitude of the signal under scrutiny. To more effectively detect circuit faults, relative and adaptive error thresholds are presented in [19, 20, 21, 14, 13]. Their error threshold can be written as:

$$V_\epsilon = k \cdot V_{sig} + V_{gb} \quad (1)$$

where k is the proportionality constant between V_ϵ and original circuit output V_{sig}. And V_{gb} is the guardband as discussed in [24, 25]. As mentioned early, the window comparator is time-shared to test different sections of the circuit. To enhance fault detection capabilities, the proportionality constant k used to determine comparator error threshold may need to be attuned to the different characteristics of the sub circuits under tested. Hence, window comparators with programmable adaptive error thresholds are preferred in online testing reconfigurable analog circuits.

2.3 Programmable Adaptive threshold

The proposed adaptive error threshold is shown in Figure 2. When its input signals are large, the window comparator uses the relative error threshold scheme. If the window comparator experiences small input signals, it switches to the constant error threshold method. By adaptively selecting error thresholds, the proposed window comparator will efficiently detect circuit faults no matter input signals being large or small.

For the convenience of discussion, we assume input signals are centered at the signal ground level V_{sg} and the maximum peak-to-peak value of the input is $2 \cdot V_A$, where V_A is the maximum magnitude of the signal. We refer to the region that the comparator has a constant error threshold as the *flat band region*. The voltage, V_F, at which the window comparator leaves the flat band region is called *flat band voltage*. The ratio of V_F to V_A is called *flat band ratio* and denoted by symbol $\mathcal{R}$. In addition, the comparator error threshold in the constant threshold region is defined as the minimum error threshold V_ϵ^{min}. The slope of the error threshold curve in the relative error threshold region is k. To meet the programmability requirement discussed in Section 2.2, parameters $\mathcal{R}$, V_ϵ^{min} and k, which characterize the comparator threshold adapting schemes, should be digitally programmed. A comparator design that implements the proposed programmable adaptive error threshold is discussed in the next section.

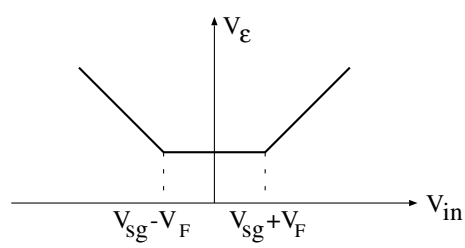

Figure 2. Adaptive threshold.

3 Proposed Window Comparator

The proposed design consists of an adaptive biasing circuit and a checker circuit whose error threshold can be programmed through its biasing current and device ratios.

3.1 Checker circuit

The checker circuit, as shown in Figure 3, is comprised of a differential input pair and four current mirrors. Transistors N_1 and N_2 constitute the differential pair. PMOS devices $P_1 \sim P_6$, which have the same size, implement two sets of PMOS current mirrors. Transistors N_4 and

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N_7, N_5 and N_6, realize two NMOS current mirrors with a current gain of m (the size of N_6 and N_7 is m times larger than that of N_4 and N_5). Assume the current flowing through N_3 is I_b. When both checker inputs are at the same level, N_1, N_2, N_4, N_5, and $P_1 \sim P6$ are in their saturation regions; and all the currents flowing through these transistors are $\frac{I_b}{2}$. N_6 and N_7, working in their linear regions, pull voltages at nodes A and B close to ground, driving the checker output to logic *1*.

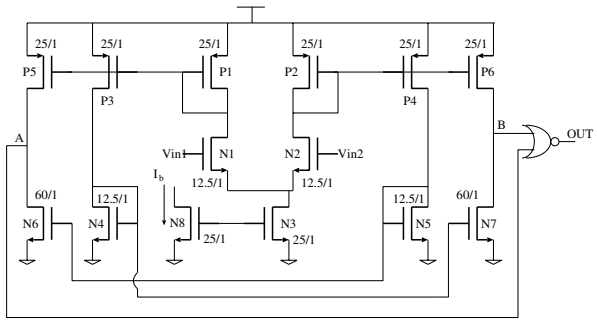

Figure 3. Proposed comparator sub-circuit.

Without losing generalities, assume checker input V_{in1} becomes larger than input V_{in2}. Consequently, currents flowing through N_1 and N_2 become $\frac{I_b}{2} + i$ and $\frac{I_b}{2} - i$, where i is the current variation caused by the input difference. When $\frac{I_b}{2} + i > m \cdot (\frac{I_b}{2} - i)$, the voltage at node A is pushed close to V_{DD} and, hence, the checker output switches to logic *0*. Assuming that I_{DS} and V_{GS} relations of N_1 and N_2 follow the perfect square-law, the checker error threshold can be derived as:

$$V_\epsilon = \sqrt{\frac{2 \cdot I_b}{\mu_n \cdot C_{ox} \cdot (W/L)_{N1,2}}} \cdot \sqrt{1 - \sqrt{1 - (\frac{m-1}{m+1})^2}} \tag{2}$$

where μ_n is the carrier mobility; C_{ox} is the transistor gate unit capacitance; and $(W/L)_{N1,2}$ is the size of N_1 and N_2.

The above equation shows that the comparator threshold can be adjusted by varying the value of m. A modified comparator circuit with programmable m values is shown in Figure 4. In the modified design, programmable current mirror (PCM) circuits replace the simple current mirrors ($N_4 \sim N_7$) used in the original design. The output branch of a PCM circuit consists of five current sink paths. Three of them can be turned on or off depending on digital signals Q_1,Q_2,Q_3, which represent a 3-bit thermometer code. The other two paths are always on to keep the minimum value of m as 2. A binary to thermometer code encoder converts two digital programming inputs to thermometer code Q_1,Q_2,Q_3. Assume all the transistors in PCM circuits have the same size, *m* can be programmed from 2 to 5. Consequently, the comparator error threshold can be scaled by factors ranging from 0.24 to 0.5.

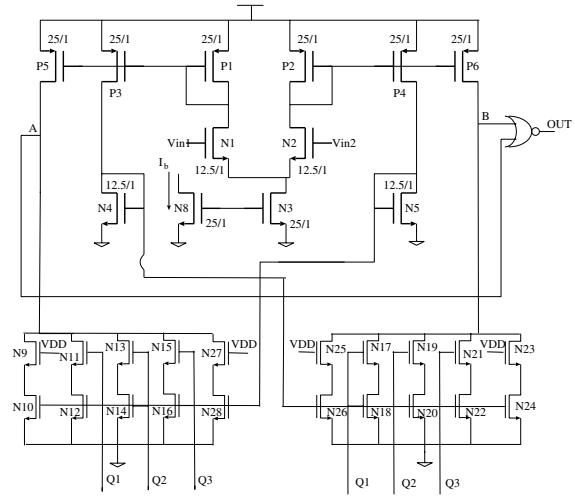

Figure 4. Modified comparator sub-circuit.

3.2 Programmable adaptive biasing circuit

Equation (2) also indicates that the checker error threshold is proportional to the square root of its biasing current. To achieve the adaptive error threshold shown in Figure 1, the biasing current should be proportional to the square of the input magnitude when the input is in the relative error threshold region. When the input is in the constant threshold region, the biasing current should be a constant. The proposed biasing circuit is given in Figure 5. It includes three current-generating blocks, labeled as U_1, U_2, and U_3. Transistors M_{16}-M_{30} generate the output biasing current according to the following equation.

$$I_b = \begin{cases} I_{min} & \text{for} \quad V_{sg} - V_f < V_{in} < V_{sg} + V_f \\ w \cdot I_p & \text{for} \quad V_{in} < V_{sg} - V_f \\ w \cdot I_n & \text{for} \quad V_{in} > V_{sg} + V_f \end{cases} \tag{3}$$

where I_p and I_n are output currents of U_1 and U_2, respectively. w is the scaling factor that is controlled by programmable inputs a and b. When checker input V_{in} is within the *flat band region*, $w \cdot I_p$ (or $w \cdot I_n$) are smaller than I_{min}. In this case, transistor M_{15} will drain current to make sure $I_b = I_{min}$. Hence, the checker has a constant error threshold.

If V_{in} is greater than signal ground level V_{sg}, M_8 in U_2 is off and M_1 in U_1 conducts current. After V_{in} leaves the flat band region, $w \cdot I_n$ becomes larger than I_{min}. Subsequently, M_{15} is off and $I_b = w \cdot I_n$. In the design, I_Q is very small and all the transistors in U_1 are in their saturation regions. Thus, I_b, which is the same as I_{DS1}, can be derived as:

$$I_b = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{w \cdot (W/L)_{M1}}{1 + \frac{1}{A} \cdot \sqrt{\frac{(W/L)_{M1}}{(W/L)_{M2}}}} \cdot (V_{in} - V_{sg} - \frac{V_t}{A})^2 \tag{4}$$

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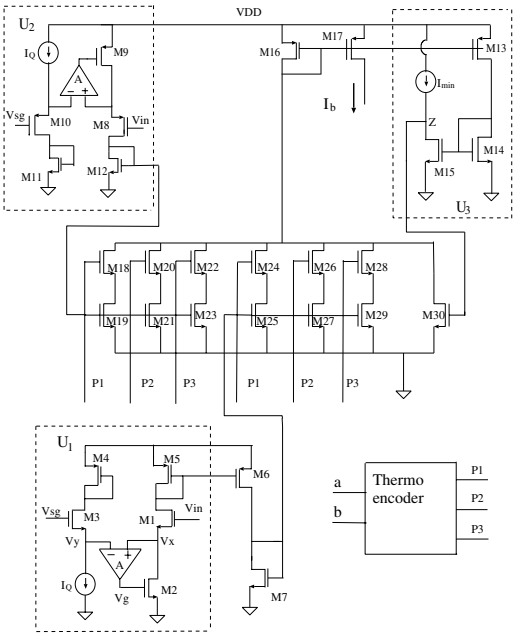

Figure 5. Proposed adaptive biasing circuit.

where V_t is the threshold of MOS devices and A is the gain of the amplifier used in U_1. Ignoring the term of $\frac{V_t}{A}$ in the above equation, the biasing current becomes proportional to the square of the input magnitude ($V_{in} - V_{sg}$). As a result, the checker has relative error thresholds. When V_{in} is smaller than V_{sg} and out of the flat band region, the biasing current I_b, which will be generated by U_2, is also proportional to the square of the input signal magnitude to implement relative error thresholds.

The programmability of the biasing circuit is realized by controlling the scaling factor w. A binary to thermometer code encoder circuit converts 2-bit programming inputs a and b to 3-bit thermometer code P1,P2, P3, which control the status of the current sinking paths in the PCM circuits. When a=0 and b=0, all three programmable current sinking paths are off. The biasing current becomes independent of U_1 and U_2 outputs. Thus the comparator circuit has a constant error threshold. Note that varying w values changes both comparator threshold gain and flat band ratio, because a large w value will cause $w \cdot I_n$, or $w \cdot I_p$ exceeds I_{min} early, and resulting a small flat band ratio.

4 Experiment Results

4.1 Simulation results

Circuit simulation has been conducted to study how the optimal comparator error thresholds should be adjusted for different sections of the CUT. An experiment circuit used in this study is a third-order chebyshev low pass filter circuit, whose schematic is shown in Figure 6. The passband of the filter is 10kHz. We also partition the circuit into four different sections, and assume that a reconfigurable testing module sequentially tests the partitioned sections.

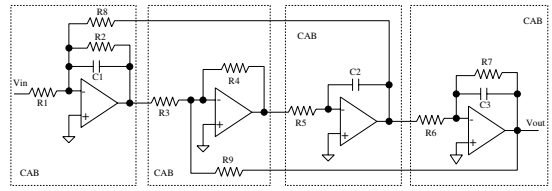

Figure 6. Leapfrog filter.

To determine the optimal comparator error threshold for a given circuit section, circuit simulation (e.g. Monte Carlo simulation) can be performed to find the maximum difference between the outputs of the original circuit and its duplication due to parasitics and circuit mismatches. For the reason of simplicity we assume each component in the circuit can vary by 0.5% of its ideal value due to process imperfections. Then, we identify the worst-case component values that lead to the maximum signal difference. To reduce simulation time, we use an amplifier macromodel in the simulation. The key parameters assigned to the amplifier model are summarised in Table 1.

Table 1. Opamp macromodel parameters.

Opamp parameters	Values
Low frequency gain	80dB
Unit-gain frequency	10MHz
Common mode rejection ratio	70dB
Input offset voltage	4mV
Slew Rate	$20V/\mu s$
Settling time (0.1%)	$0.5\mu s$
Power supply	3.3V
Output swing range	$0.18V \sim 3.1V$

With allowed component value variations, the maximum signal difference ΔVs for the second and the fourth sections of the filter circuit are plotted in Figure 7. In the simulation, we vary the magnitude of the filter input such that the signal magnitude at the output of the sub circuits (sections) are also changed. Figure 7 clearly shows that the signal difference ΔVs are proportional to the magnitude of the signals under scrutiny. This justifies the need for the adaptive error threshold scheme. The plot also shows that the relations between ΔV and the magnitudes of the signal under scrutiny for the second and the fourth sections are different. It explains the need for programmability in window comparator circuits.

With using the leapfrog filter as an example circuit, we also compared the fault detection capabilities when using the proposed comparator and a conventional one with constant error threshold. The constant error threshold value is

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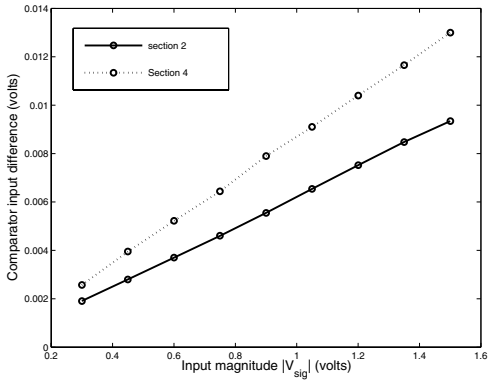

Figure 7. Difference between the outputs of the CUT and its replication.

selected according to the maximum ΔV value. The proposed comparator used in the experiment has an adaptive error threshold that fits the ΔV behavior for the CUT. In the experiment, we inject parametric faults at component C_1 in the first section of the filter circuit. Figure 8 shows how the detectable faults vary with different filter input levels. The reported detectable faults are described by their variations from the normal component value, which is 255 unit capacitances. Thus a smaller value indicates a less severe fault. It shows fault detection capability degrades for both the comparators when the filter circuit has a smaller input. This is mainly due to adding the guard-band component in the error threshold. Nevertheless, the experiment results clearly show an improved fault detection capability is achieved by using the proposed comparator.

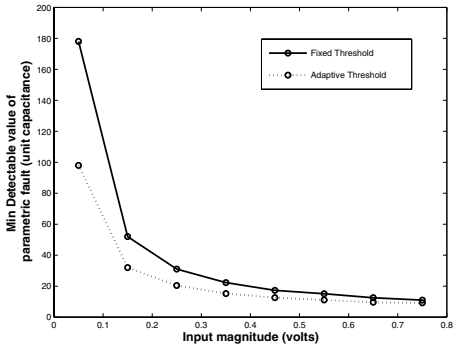

Figure 8. Minimum detectable fault at C_1 with different filter input levels.

4.2 Measurement results of the fabricated comparator

The proposed comparator has been implemented using a 0.18μ CMOS technology. Transistor sizes used in the checker circuit are given in Figure 3. Single-stage differential amplifiers [26] are used in the adaptive biasing circuit. The design requires a single 3.3V power supply and the signal ground level is 1.65V. Figure 9 shows a testing result of the fabricated chip. The inputs of the checker are two sinusoidal signals V_{in1} and V_{in2} with the same magnitude, frequency, and phase. V_{in1} is centered at the signal ground level, while V_{in2} is shifted down by 160 mV. Input V_{in1} is also connected to the biasing circuit (as is Vin shown in Figure 5) to control the biasing current. The square-like wave in Figure 9 shows that this difference is detected by the checker (checker output is logic 0) when the signal values are close to the signal ground level. When the inputs are close to their peak values, the same difference is ignored by the checker due to its increased error threshold.

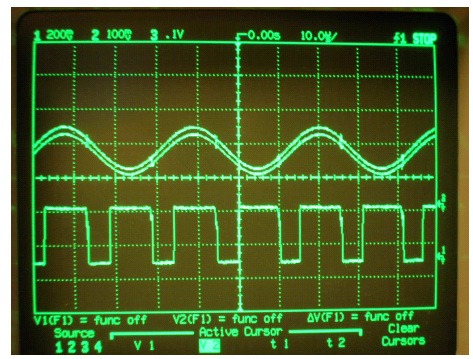

Figure 9. Captured oscilloscope display.

The programmability of the proposed design is also verified by our testing results. Figure 10 shows measured comparator thresholds at different input levels. The four curves in the figure correspond to the realized comparator error thresholds with different digital values applied to the programmable inputs a and b of the biasing circuit (depicted in Figure 5). When both a and b are logic 0, a constant error threshold is realized seen as a flat straight line over the entire input range. With other digital *ab* values, the proposed adaptive error threshold scheme is observed.

5 Concluding Remarks

This paper discusses the optimal error threshold for window comparators used in analog online testing. A window comparator with programmable adaptive error threshold is presented. Experiment results demonstrated that improved fault detection capabilities can be achieved by using the proposed comparator. The proposed comparator has been designed and fabricated using a 0.18μ CMOS technology. Measurement results of the fabricated chip are also presented.

Although the proposed design is more complex compared to previous designs, its programmabilty will allow a single comparator to be time-shared to test different sec-

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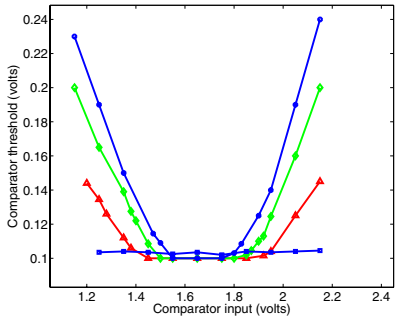

Figure 10. Programmable adaptive error thresholds.

tions of the CUT with a better fault detection capability. The comparator itself can also be tested using simple built-in-self-testing (BIST) circuits. A simple approach is to feed the comparator inputs with ramp signals and use counters to monitor when the comparator output switches. Combining this BIST feature, the comparator will be suitable for implementing online testing circuits on analog reconfigurable platforms.

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