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Glitch Control with Dynamic Receiver Threshold Adjustment

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Glitch Control with Dynamic Receiver Threshold Adjustment

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Abstract

A novel method to treat crosstalk induced glitches on local interconnects is presented. Design irregularities and manufacturing defects in system-on-chip interconnects may result in spurious electrical events that impact the reliability of the interconnect infrastructure. Conventional repeater insertion methods prove to be space and power demanding. The proposed method acts by dynamically adjusting the threshold voltage of the receiving gate without breaking the line in multiple segments. A comparative study is presented that supports the applicability of the approach.

1. Introduction

In deep sub-micron, technology scaling and manufacturing defects such as proximity effects have increased the design vulnerability to crosstalk. The latter may easily induce additional delay and impose electric transitions (glitches) on a line that could result in functional errors. Existing literature suggests methods to deal with these issues, such as the well-known repeater insertion [1, 2, 3, 4] or others like interconnect tuning [5] and dynamic shielding [6].

In this paper we focus solely on glitch remedies keeping an eye on delay and power as important performance factors. Our objective is to resolve crosstalk instances on short interconnects where traditional repeater insertion may not be advantageous especially in the case of pronounced coupling errors.

This paper is divided in 6 sections. In Section 2 we define a generic glitch situation to which the different remedies will be applied. In Section 3 we present our proposed method. In Section 4, more details on the experimental setup are provided. In Section 5, we illustrate the results of our comparative study and the paper is concluded in Section 6.

2. Problem Definition

The purpose of this research is to apply a receiver-end based correcting mechanism for coupling induced glitches appearing on short lines. Figure 1 presents a typical case of coupling effects on a line, due to the action of one or more aggressors. The present coupling is of capacitive nature and was based on the TSMC 0.18 μm CMOS technology. The circuit used in the simulation is shown in Figure 2. An extracted 500 μm long and 0.28 μm wide metal layer 3 line is used. The proposed methodology is compared with the known from the open literature approach of buffer insertion. In order to eliminate the glitch with the use of buffers we separate the line into smaller pieces (at least 100 μm long each) and insert repeaters between each part.

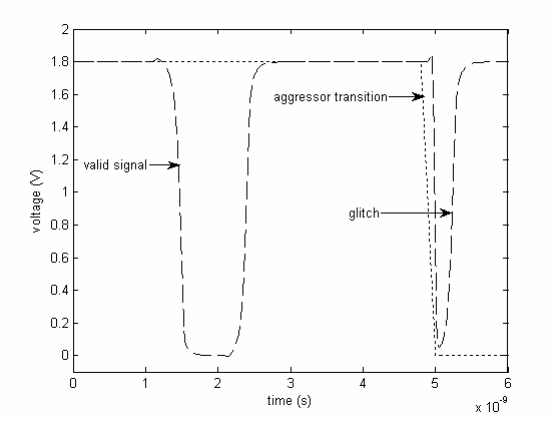

Figure 1: Generic Glitch

The paper aims to offer a solution capable of solving the following problem. Due to coupling effects for a particular circuit topology, a transition on a nearby aggressor line results in a glitch on a quiet victim line.

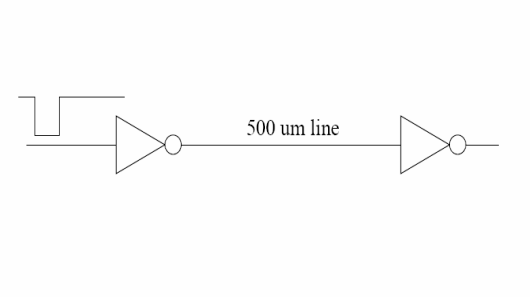

Figure 2: Driver Receiver Circuit – Conf (I)

Coupling effects are an ongoing research issue and for comparison purposes we consider scenarios where the line is more vulnerable. Such a case is when an arbitrary capacitive coupling occurs at the end of the line. The coupling is assumed to be caused by two identical aggressors (as in [4]) affecting the line equally, each having a coupling capacitance of 600 fF with respect to the victim line. Width of the glitch is 450 ps.

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We present a new concept that minimizes crosstalk induced glitches through dynamically adjusting the threshold of the receiving gate. Crosstalk effects are artificially generated using simple circuits. For the completeness of our comparisons the considered circuit setup involves severe coupling as it is expected to be the case in future deep submicron technologies. Thus, we can include the expected effects of design errors and manufacturing defects imposing additional hazards that ideal simulators do not account for. Inclusion of these cases does not invalidate the proposed research. On the contrary, it stresses its significance in modern IC design where proximity effects and other irregularities impact irreversibly circuit performance. Also, with the continuous device size scaling, the crosstalk effects are expected to be more severe and, consequently, there will be more need for the proposed circuit.

3. Dynamic Receiver Threshold Adjustment

The proposed method is proved to be very effective for treating a crosstalk induced pulse on a victim line determined by the circuit topology. This technique is more suitable for short local interconnects as Figure 3 shows. It is based on a typical driver-receiver configuration and thus only a single segment of line is involved. For longer lines, traditional repeater insertion proves to be a more robust design strategy since a single driver could not drive the line load by itself with the same efficiency.

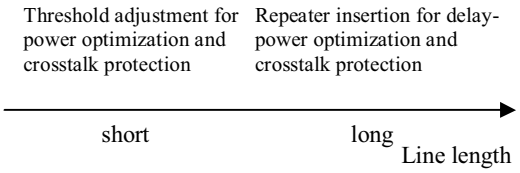

Figure 3: Operation of the proposed circuit

The goal is to synchronize the corrective circuit with the aggressor so that it operates only when the aggressor threatens the validity of the data on the victim line. This on line testing circuit requires physical connection between the aggressor and the victim. The basic concept is to adjust the threshold voltage of the receiver inverter on the victim line so that the hazard is ignored. Hence, a rising glitch on the victim line would require an upwards adjustment of the threshold voltage in the receiver and vice versa.

The basic circuit to achieve this is shown in Figure 4. At the end of the line, before our main receiver inverter we have two essential pieces of circuitry: a small size inverter and a circuit interacting with the aggressor(s). Signals $\mathbf{a_d}$ and $\mathbf{a_i}$ are the delayed and inverted signals coming from the first aggressor and since we have assumed two aggressors in this case, signals $\mathbf{b_d}$ and $\mathbf{b_i}$ are the delayed and inverted signals coming from the other one. These two signals required from each aggressor are generated by using one and two minimum size inverters in series to produce the inverted and delayed signal respectively. The additional capacitive load caused by these inverters is minimal and hence the impact on the aggressors is very small.

Consider simultaneous rising transitions in the aggressor lines when victim line is at low logic. This will result in a rising glitch on the victim. For rising transitions, the inverted signals being generated will be falling transitions. We adjust the delay for the aggressor signals so that they are also maintained at low logic for some time interval Dt as shown in Figure 5. As a result, the pMOS network in Figure 4 will conduct, shifting thus the threshold voltage of the circuitry at the end of the line upwards, in order to ignore the rising glitch on the victim line.

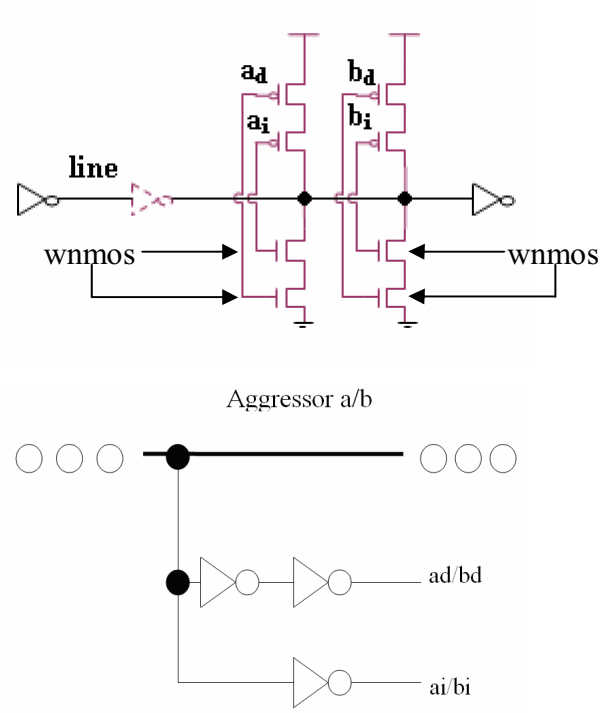

Figure 4: Dynamic threshold adjustment circuit

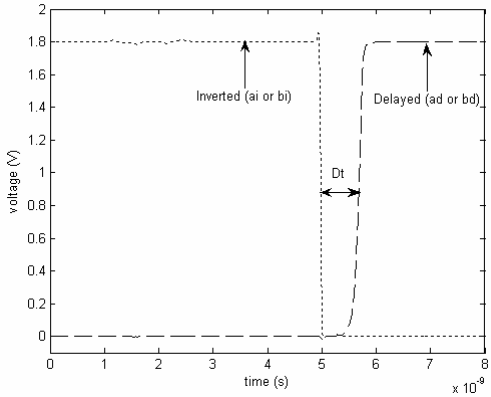

Figure 5: Inverted and delayed aggressor signal

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Similarly, in the case of a falling glitch, opening nMOS will adjust the threshold downwards. The time of operation for this circuit will depend on time Dt and can be adjusted to treat even wider glitches if desired up to a certain extent. A DC analysis illustrated in Figure 6 describes the threshold adjustment with varying the size of the transistors in the generic circuit described in Figure 4.

4. Experimental Setup

We overall try to eliminate the coupling effect using, besides the proposed technique, five different circuit configurations based on the conventional repeater insertion approach. The generic sheme for repeater insertion is depicted in Figure 7. We define the following circuit cases: (I) no repeater inserted (equivalent to Figure 2), (II) one repeater inserted, (III) two repeaters inserted, (IV) three repeaters inserted and (V) four repeaters inserted. For each of the cases (I), (II), (III), (IV) and (V) we assume hence that repeaters are used every 500, 250, 125, 167 and 100 μm long lines respectively. In each circuit configuration, all inverters are of identical size and they all scale up or down uniformly as presented in existing literature [1, 2, 4]. The objective is to treat the crosstalk with the minimum penalty in delay, power dissipation and effective transistor area. Metal layer 3 lines of 500, 250, 167, 125 and 100 μm length and 0.28 μm width have been extracted based on the TSMC 0.18 μm CMOS technology using Cadence Assura tool. All gate widths in all circuits for pMOS transistors are considered to be 2.5 times the widths of the corresponding nMOS ones.

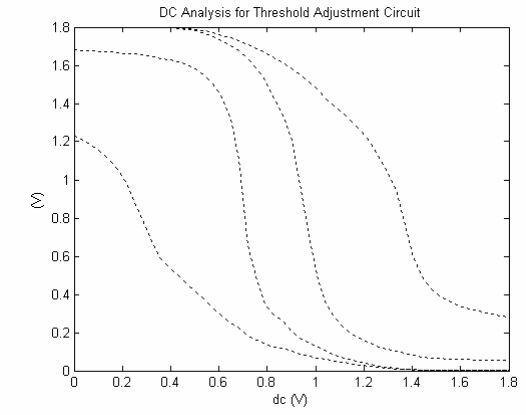

Figure 6: DC Analysis for circuit in Figure 4

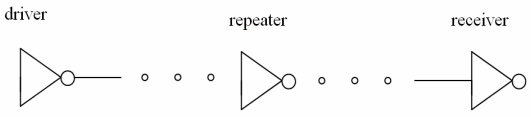

Figure 7: Generic scheme for repeater insertion

5. Results and Discussion

In this section, we present experimental results for treating the glitch described in section 2 with the five different circuit cases (I), (II), (III), (IV) and (V) as well as with the proposed circuit. First we present the treatment of the glitch using the dynamic threshold adjustment circuit described in section 3. Each of the remaining configurations then is studied and presented separately. For each one we start off with a delay optimized sizing of the inverters as illustrated in Figure 8 and observe its behavior with respect to the introduced hazard. Delay and dissipated power are plotted for each configuration as a function of the crosstalk amplitude. Delay is measured for the victim line when the aggressors are quiet. The measured power in all cases includes power consumed by both the aggressors and the victim.

The optimization was performed experimentally running parametric analyses. From this graph, it is obvious that circuit (III) contains the optimal size & number of repeaters. After optimizing for each circuit, continuous uniform scaling is performed for treating the glitch at the receiver output until a 95% reduction has been achieved. In section 6, we show how these results vary for different levels of glitch reduction (sweeping glitch reduction).

5.1 Dynamic threshold adjustment

For the proposed method, the results are shown below. We said that this is a method based on a driver-receiver configuration. Hence, the driver and the receiver are delay optimized as in the case of circuit (I). In Figure 9, we show how our method performs by adjusting the transistor sizes of the circuit in Figure 4. We see for relatively small sizes, we can drop the crosstalk significantly. Glitch at the output of receiver is reduced by 95% with a delay of 460 ps and 10.206 pW power consumption.

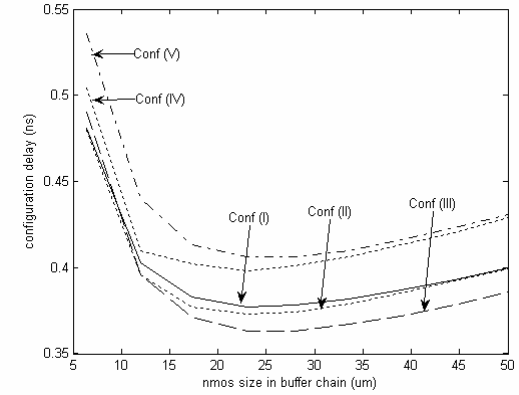

Figure 8: Delay optimized circuits (I) to (V)

5.2 Configuration (I)

For this circuit, the assumption is that repeaters are inserted every 500 μm (hence, none inserted in this case). In Figure 10, we show the output of the

receiver inverter in circuit (I) before and after scaling up the inverters. The dotted line is showing the output signal in the delay optimized circuit before scaling. In order to reduce the crosstalk by 95%, which is the metric used here, we roughly have to scale up the inverters by 8.5 times.

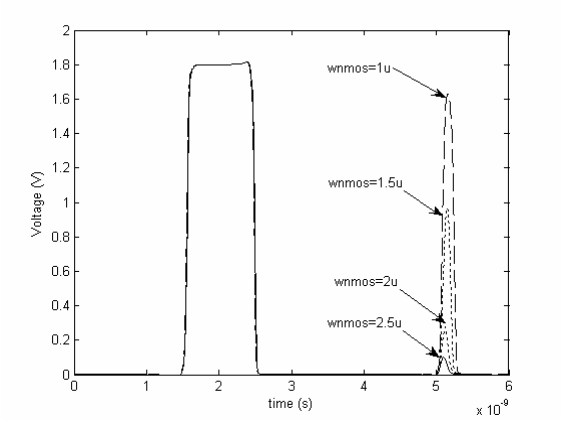

Figure 9: Dynamic Threshold Adjustment

Delay and power are given below in Figure 11 as a function of the achieved crosstalk reduction. Delay (631 ps) is increased by 37% and power (60.849 pW) has increased by 496% in comparison with the proposed circuit.

5.3 Configuration (II)

In this case repeaters can be inserted every 250 μm (hence, insert one repeater). Figure 12 shows the output signal before and after scaling up the inverters. In order to drop the glitch by 95%, we have to enlarge our inverters 4.5 times.

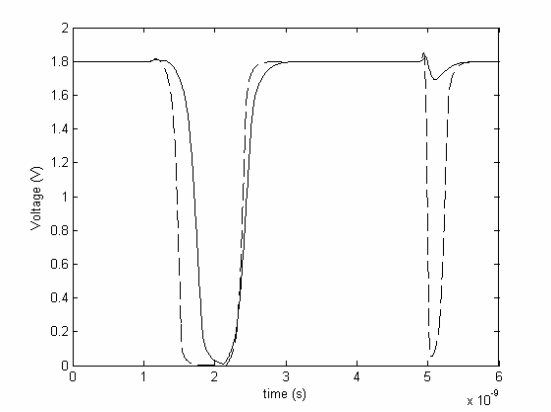

Figure 10: Circuit (I) before and after scaling

Figure 13 gives the delay and the power dissipation as a function of the crosstalk amplitude. Delay (511 ps) has increased by 11% and power (34.893 pW) has increased by 240% compared to our adaptive circuit.

5.4 Configuration (III)

In this case, repeaters are added every 167 μm (so, 2 repeaters are added). Output signal before and after scaling are in Figure 14. Delay and power dissipation as functions of the dropped crosstalk are in Figure 15. Note that by increasing the number of repeaters in the delay optimized circuits (I) to (V), the crosstalk amplitude for the delay optimized configuration drops progressively but not considerably to allow us to avoid scaling.

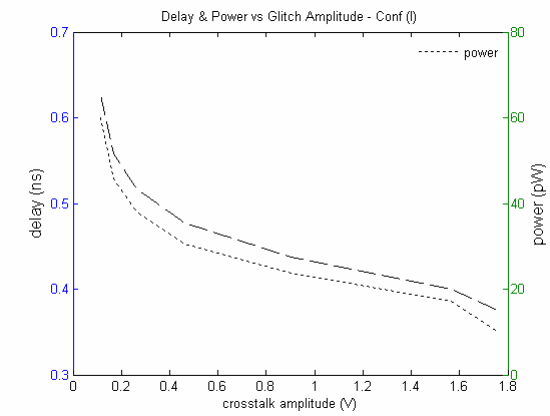

Figure 11: delay & power vs. crosstalk for (I)

For reducing the glitch level by 95% a 5 times scale up is required. Delay (554 ps) has increased by 20% and power (53.064 pW) has increased by 419%.

5.5 Configuration (IV)

For this circuit, we assume that repeaters are added every 125 μm (and so, overall 3 repeaters are added). Output before and after buffer sizing is in Figure 16. As always, the dotted line is the delay optimized circuit output. Also, delay and power increase are given in Figure 17.

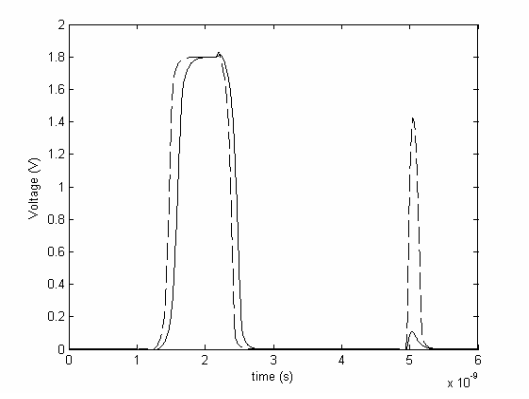

Figure 12: Circuit (II) before and after scaling

In order to eliminate 95% of the initial crosstalk, a scaling of about 4 is necessary. Delay (515 ps) has increased by 12% and power (36.297 pW) has increased by 255%.

5.6 Configuration (V)

For the last configuration, Figure 18 shows output before and after sizing. Figure 19 gives delay and power as function of the reduced crosstalk.

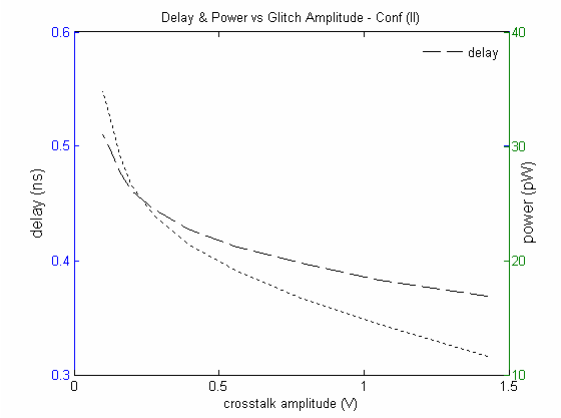

Figure 13: delay & power vs. crosstalk for (II)

In this case a 5.8 times scale up is performed. Delay (613 ps) has increased by 33% and power (64.242 pW) increased by 529%.

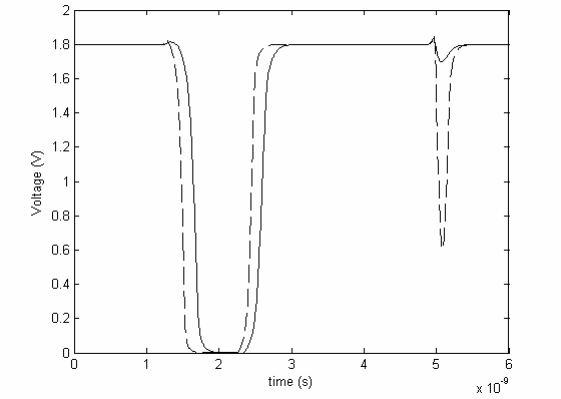

Figure 14: Circuit (III) before and after scaling

6. Concluding Remarks

In the previous repeater insertion configurations, the best performing one is configuration (II) in terms of delay and power dissipation. If the required reduction of the glitch is 95%, the two methods yield comparable delay (circuit (II) is by 51 ps slower). However, effective transistor area and power dissipation are 1.4 and 3.4 times respectively larger for circuit (II).

For different levels of crosstalk correction, the delay and the dissipated power are given from 75% (~Vt) to 95% (~Vt/4) glitch reduction in Figures 20 and 21. As far as the dissipated power is concerned, the proposed method outperforms the classic methodology. For a limited glitch reduction (~Vt), the delay of the repeater schemes is smaller but that's not enough to guarantee proper circuit operation due to the glitch amplitude.

Instead of extracted lines, RC modeling of the lines was also examined for confirming results. Electrical parameters used for a Metal layer 3 line were taken directly from MOSIS wafer acceptance tests and the presented trend was confirmed.

Receiver threshold adjustment is proposed for short local interconnects. In addition, the presented method is convenient for glitches over 400 ps duration. On the other hand, for narrow glitches up to 150-200 ps width, a small receiver inverter (having slow response) can be inserted in front of the main receiver inverter. So, we manage to cut off successfully the incoming glitch with a small delay penalty (~75 ps).

Further more, this method can prove to be particularly useful in Networks on Chips in the case of routing over embedded IP protected cores. In such a case, no repeaters can be added. Therefore, provided that a wide line can be used for reducing line resistance, a driver-receiver scheme can be adopted for increased crosstalk protection based on the presented method.

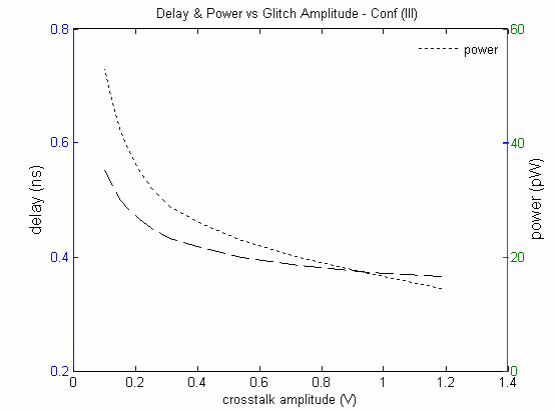

Figure 15: delay & power vs. crosstalk for (III)

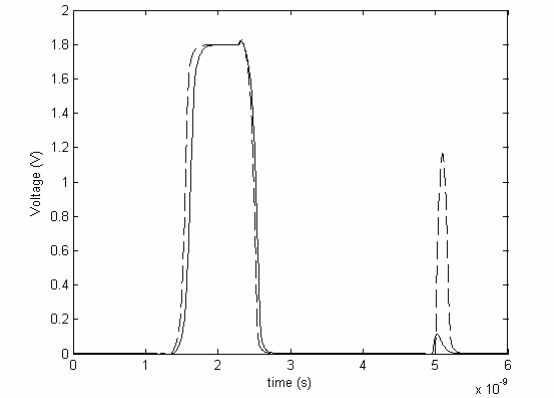

Figure 16: Circuit (IV) before and after scaling

Lastly, an alternative application of the dynamically adjusted receiver threshold could be in conjunction with the repeater insertion method in order to reduce the overall number of repeaters added on a line.

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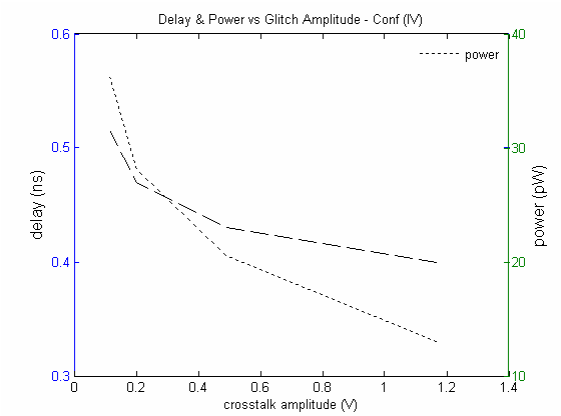

Figure 17: delay & power vs. crosstalk for (IV)

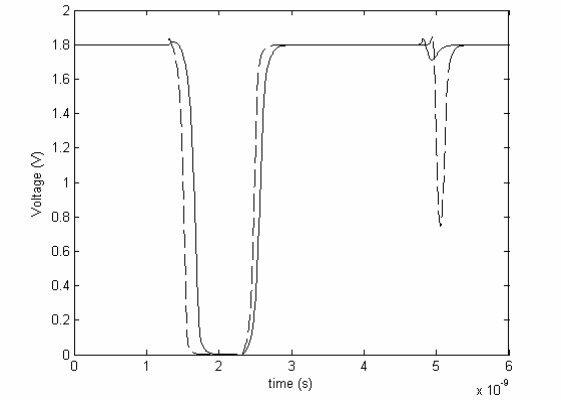

Figure 18: Circuit (V) before and after scaling

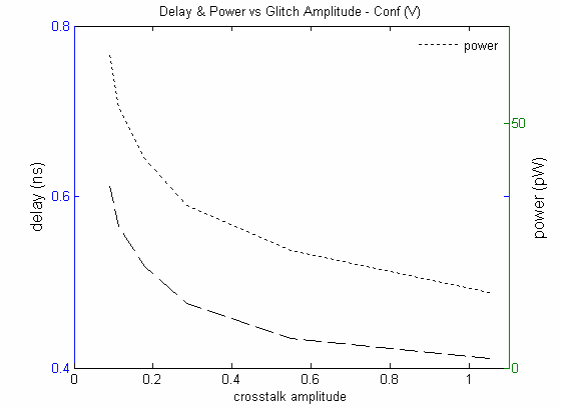

Figure 19: delay & power vs. crosstalk for (V)

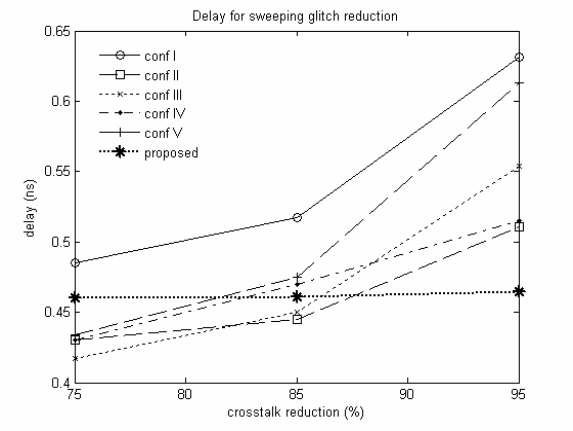

Figure 20: delay for sweeping glitch reduction

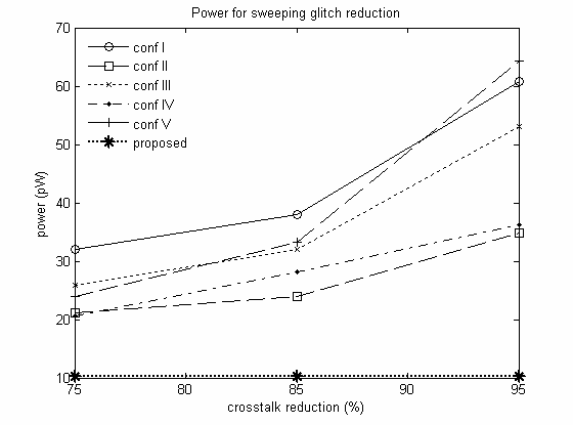

Figure 21: power for sweeping glitch reduction

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