3-2006

Design of Window Comparators for Integrator-Based Capacitor Array Testing Circuits

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Published in Laknaur, A., & Wang, H. (2006). Design of window comparators for integrator-based capacitor array testing circuits. Proceedings of the 7th International Symposium on Quality Electronic Design (ISQED'06). doi: 10.1109/ISQED.2006.47

Design of Window Comparators for Integrator-Based Capacitor Array Testing Circuits

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Abstract

This paper investigates the impact of window comparator threshold variations on the performance of integrator-based programmable capacitor array (PCA) testing circuits. It presents two window comparator designs that take different approaches to address the problem of comparator threshold variations in PCA testing. The first comparator design utilizes a fully symmetric circuit structure to achieve small threshold deviations. The second design relies on increasing testing time to reduce the effect of comparator threshold variations. Experimental results are presented to compare the performance of the two design approaches.

1. Introduction

Due to their numerous advantages, reconfigurable analog circuits have attracted significant research interests and development efforts. In many reconfigurable analog circuits, programmable capacitor arrays (PCAs) are used as an essential mechanism to configure circuit parameters. The popularity of using PCAs comes from the fact that PCAs can be easily programmed with high accuracy and large ranges.

An n-bit PCA has 2^n possible configurations. Exhaustively testing each configuration leads to lengthy testing processes. To address this problem, PCA built-in-self-testing (BIST) circuits, consisting of switched-capacitor (SC) integrators and window comparators, have been proposed [3] along with the study of the impact caused by non-ideal effects of SC integrators on the performance of PCA BIST circuits. However, window comparators were assumed as ideal components in the previous study. This work investigates how window comparator threshold deviations affect the efficiency of integrator-based PCA BIST circuits.

Previously, various window comparators have been proposed for analog testing purposes. The circuit presented in [11] utilizes two operational amplifiers (op-amps) and a set of resistors which govern comparator threshold voltage. Comparators in [8, 5] are designed to take differential inputs and monitor their common mode levels. Both circuits utilize differential input pairs as pre-amplifiers and the outputs of the pre-amplifiers are digitized by inverters. Comparators in [1, 2] are based on a folded cascoded op-amp topology. Asymmetric differential pairs are intentionally used at the input stage for introducing input offset voltage, which is translated into comparator threshold. In most of the previous work, fewer efforts were devoted to minimizing comparator threshold variations. This paper addresses the lack of such discussion in window comparator design, and presents two comparator circuits that take different approaches to address the effects of comparator threshold variations on PCA testing.

The rest of the paper is organized as follows. Section 2 explains PCA implementation and summarizes its fault models. Integrator-based PCA testing techniques are also explained in this section. Section 3 discusses the impact of comparator threshold variations on the efficiency of integrator-based PCA testing circuits. A case study is performed to show how to minimize the impact of comparator threshold deviations during PCA testing. Section 4 presents two window comparator circuits for being used in PCA BIST circuits. Experimental results are presented in Section 5, and the paper is concluded in Section 6.

2. Preliminaries

2.1 PCA fault models

Normally an n-bit PCA contains n binary weighted capacitor branches connected in parallel. A branch is made up of a group of identical capacitors, which are referred to as unit capacitors. The different parametric faults that could occur in a PCA are explained below. Leakage paths may exist in the isolation layer between the two terminals of a unit capacitor. This leads to a leakage fault whose fault model is given in Figure 1(a). Due to excess metal or dust, two interconnects ideally isolated may become connected through a

†This material is based upon work supported by the National Science Foundation under Grant No. 0448357.

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resistive path. This is called bridge fault and its fault model is shown in Figure 1(b). Switches used in PCAs are normally implemented using transmission gates. Their switching characteristics can be deteriorated by excessively large on-resistance or excessively small off-resistance [7]. These two types of faults are referred to as large on-resistance fault and small off-resistance fault (as in Figure 1(c) and (d), respectively). For more discussion of PCA faults, please refer to literature [3].

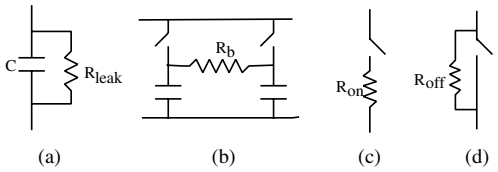

Figure 1. PCA parametric faults.

2.2 Integrator-based PCA BIST circuit

A previously proposed integrator-based PCA BIST circuit [3] is depicted in Figure 2. Assuming $C_A = C_B$ and both fault-free, the output of the integrator should be ideally at signal ground level as the net charge transferred from C_A and C_B to C_f is zero during each integration cycle. Otherwise charge will be accumulated at capacitor C_f, resulting in the integrator output to deviate from signal ground level. During the testing process, the integrator output is fed to a window comparator after a fixed number of integration cycles. If the difference between signal ground and the integrator output is within the range of $[-V_\epsilon, V_\epsilon]$, where V_ϵ is referred to as the window comparator *threshold*, the comparator output is logic **1** to indicate that the circuit is fault-free and else, is logic **0** marking the occurrence of faults.

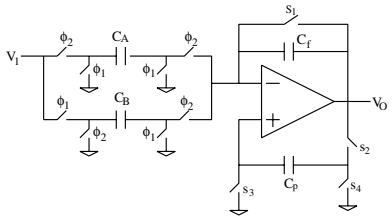

Figure 2. Integrator-based PCA BIST circuit.

3. Impact of window comparator threshold variations

Practically, the integrator output in fault-free scenarios will not be exactly at signal ground level, due to non-ideal circuit effects, such as channel charge injection and parasitic capacitance. Typically, the maximum difference between signal ground and the integrator output in fault-free scenarios can be estimated (e.g. by Monte Carlo or corner simulation). For the convenience of discussion, we use V_k^{max} to denote the largest possible integrator output in fault-free scenarios after k integration cycles. Ideally, window comparator threshold V_ϵ can be selected to equal V_k^{max} when designing PCA BIST circuits. However, due to process variations, realized comparator thresholds are random values which are distributed around the designed threshold. As these type of problems are typically studied using statistical distributions, they are modeled by *mean values* and *standard deviations*. If the comparator is designed such that the mean value of its threshold, denoted as $\bar{V}_\epsilon$, is equal to V_k^{max}, the occurrence of process variations that lead to smaller V_ϵ will result in good devices being labeled as faulty.

To address the above problem, $\bar{V}_\epsilon$ can be selected slightly larger than V_k^{max}. This reduces the likelihood of throwing good devices as bad components, but degrades the capability of detecting parametric faults. How to optimally select $\bar{V}_\epsilon$ is a subject of yield analysis or product profitability study. In this work, we take a simple approach that selects $\bar{V}_\epsilon$ larger than V_k^{max} by $3 \cdot v_\sigma$, where v_σ is the standard deviation of the comparator threshold. Assuming that the variation of the comparator threshold follows Gaussian distribution, this approach guarantees that the possibility to label a good device *faulty* is smaller than 0.3% [6]. To more effectively explain how comparator threshold variations affect the efficiency of integrator-based PCA testing circuits, we conduct a case study to show the relation between standard deviations of comparator threshold and detectable ranges of large on-resistance faults. A large on-resistance fault increases circuit RC delay and, consequently, prevents the capacitor from getting fully charged (or discharged) during the corresponding clock phase. As a result, less charge is transferred from the faulty input branch to the integrator feedback capacitor. The same effect can be achieved by eliminating the large on-resistance and reducing the capacitor value. Therefore, a large on-resistance fault can be modeled by a fault-free circuit with an attenuated capacitor as shown in Figure 3.

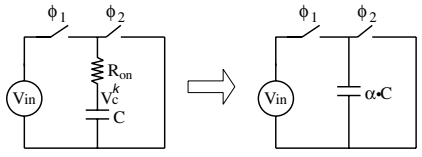

Figure 3. Modeling large on-resistance faults by capacitor attenuation.

The *attenuation factor* α, which is the ratio of the reduced capacitor value over its original value, is derived as follows. We use V_c^k to denote the voltage across capacitor C in Figure 3 after ϕ_1 phase of the kth clock cycle. Then,

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we have the relation:

$$V_c^k = V_{in} \cdot (1-\mu) + V_c^{k-1} \cdot \mu^2 \quad (1)$$

where $\mu = e^{\frac{-T}{2 \cdot R_{on} \cdot C}}$ and T is the period of the clock used in the circuit. This recursive equation can be re-written as:

$$V_c^k = V_{in} \cdot (1-\mu) \cdot \frac{1-\mu^{2\cdot(k+1)}}{1-\mu^2} + V_c^0 \cdot \mu^{2\cdot k} \quad (2)$$

where V_c^0 is the initial voltage across capacitor C. μ is very small when the value of $R_{on} \cdot C$ is much less than $\frac{T}{2}$ (which is the case when we study for the minimum detectable on-resistance faults). Consequently, the above equation can be approximated as:

$$V_c^k = V_{in} \cdot (1-\mu) \quad (3)$$

During the kth clock cycle charge transferred by capacitor C can be calculated as:

$$Q = C \cdot V_c^k \cdot (1-\mu) = C \cdot V_{in} \cdot (1-\mu)^2 \quad (4)$$

Hence, the capacitor attenuation factor is:

$$\alpha = (1-\mu)^2 \quad (5)$$

Figure 4 compares the amounts of transferred charge obtained from circuit simulation and estimation. It shows that the capacitor attenuation factor accurately models the effect of R_{on} when $R_{on} \cdot C$ is relatively small.

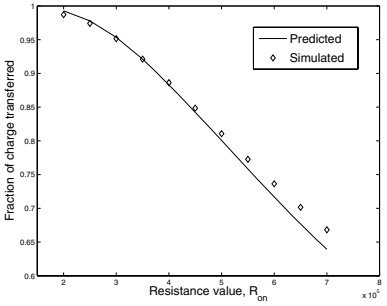

Figure 4. Comparison of predicted and simulated charge transfer.

Without losing generalities, we assume a large on-resistance fault occurs at PCA C_A in Figure 2. Therefore, C_A can be replaced by $\alpha \cdot C_A$ in circuit analysis. As a result of the fault, the net charge accumulated on C_f during one integration cycle is:

$$\Delta Q = \alpha \cdot C_A \cdot V_{in} - C_B \cdot V_{in} \quad (6)$$

The integrator output after k integration cycles can be calculated as:

$$V_k^f = \frac{\Delta Q \cdot k}{C_f} \quad (7)$$

The previous discussion indicates that the probability of detecting this fault is greater than 0.997 if $V_k^f > V_k^{max} + 6 \cdot v_\sigma$. From this inequality, we can solve the minimum detectable large on-resistant fault as:

$$R_{on} = \frac{-T}{2 \cdot C_A} \cdot \frac{1}{\ln(1-\sqrt{\alpha_{min}})} \quad (8)$$

where α_{min} is:

$$\alpha_{min} = 1 - \frac{(V_k^{max} + 6 \cdot v_\sigma)}{V_{in}} \cdot \frac{C_f}{C_B} \quad (9)$$

Assigning $C_A = C_B = 20pF$ and $C_f = 8pF$, the estimated minimum detectable large on-resistance faults are plotted in Figure 5. Note that the reported detectable faults are normalized by the maximum allowed on-resistance value R_{max}, which is defined as the maximum on-resistance value that guarantees at the end of a charging cycle the voltage across the capacitor reaching 99.9% of its ideal value. Three comparator threshold standard deviations, $v_\sigma = 10$mV, 20mV, and 40mV, are selected in the study and their corresponding detectable faults are plotted using solid, dot, and dash lines, respectively, in Figure 5. It is not a surprise to see that the fault detection capability is degraded when v_σ is large. The plot also reveals that increasing integration cycles can partially overcome the negative impact caused by large v_σ. For example, to detect a large on-resistance fault that has the value of $1.2 \cdot R_{max}$, if comparator v_σ is 10mV, only 4 integration cycles are needed in the testing process. However, if the comparator v_σ is 40mV, 14 integration cycles have to be performed to achieve the same level of fault detection capability. With the increase of integration cycles, comparator thresholds, indicated by solid lines with legends in Figure 5, have to be increased accordingly.

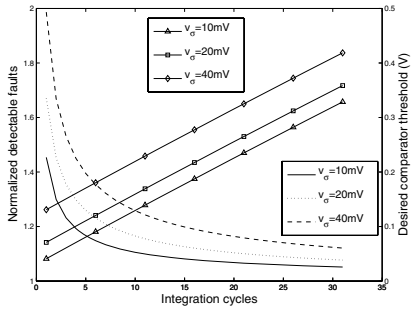

Figure 5. Detectable large on-resistance faults v.s. integration cycles.

4. Design of analog window comparators

As discussed in the previous section, excellent PCA fault detection capability can be achieved by either using com-

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parators with small threshold deviations or increasing integration cycles. The latter relaxes the requirement on comparator v_σ but results in large comparator thresholds. This section presents two comparators that fit in the above two design approaches. The first comparator utilizes a circuit topology that is similar to a fully symmetric operational transconductance amplifier (OTA). With proper biasing and device matching techniques, it has the potential to achieve very small v_σ. The second comparator is based on inverter circuits. It can easily realize large comparator thresholds but with significant deviations.

4.1 OTA-based comparator

The OTA-based comparator, as shown in Figure 6, is comprised of a differential input pair and four current mirrors. Transistors N_1 and N_2 constitute the differential pair and their tail current is provided by transistor N_3. PMOS devices $P_1 \sim P_6$, which have the same size, implement two sets of PMOS current mirrors; while, transistors N_4 and N_7, N_5 and N_6, realize two NMOS current mirrors. The size of transistors N_6 and N_7 is m times larger than that of N_4 and N_5. Assume the tail current flowing through N_3 is I_b. When both comparator inputs are at the same level, transistors N_1, N_2, N_4, N_5, and $P_1 \sim P6$ are in their saturation regions, and all the currents flowing through these transistors are $\frac{I_b}{2}$. Devices N_6 and N_7, working in their linear regions, pull voltages at nodes A and B close to ground, driving the comparator output to logic **1**. When there is a difference between the comparator inputs, currents flowing through devices N_1 and N_2 become $\frac{I_b}{2} + i$ and $\frac{I_b}{2} - i$, or *vice versa*. It is easy to see that node A or B switches to high voltage level if

$$\frac{I_b}{2} + i > m \cdot (\frac{I_b}{2} - i) \tag{10}$$

Assuming that the relation between I_{DS} and V_{GS} of N_1 and N_2 follows perfect square-law, the comparator threshold can be derived as:

$$V_\epsilon = \sqrt{\frac{I_b}{\mu_n \cdot C_{ox} \cdot (W/L)_{1,2}}} \cdot \sqrt{1 - \sqrt{1 - (\frac{m-1}{m+1})^2}} \tag{11}$$

where μ_n is the electron mobility; C_{ox} is the device unit gate capacitance; and $(W/L)_{1,2}$ is the device size of N_1 and N_2.

The proposed circuit is similar to a previous current window comparator [9] in the aspect of comparing current signals at high impedance nodes. However, the proposed circuit takes voltage signals as input, needs only one reference (instead of two as required in [9]), has a symmetric structure and several other advantages. First, the comparator threshold can be controlled by adjusting three parameters m, I_b, and $(W/L)_{1,2}$ resulting in significant flexibility during the circuit optimization phase. Second, if N_3 gate voltage V_{bias} is provided externally or by a biasing circuit whose output level can be regulated externally, the comparator threshold can be adjusted in the field. This feature can be exploited to fine-tune the comparator threshold to adapt to varying performance specifications, or to combat the effects of device aging or changing environment. Third, the fully symmetric structure of the circuit reduces the impacts of process variations on circuit performance. In addition, if proper techniques are used in the design to minimize device mismatches, the comparator threshold variation can be controlled at small values. Monte Carlo simulations have have been performed for the circuit shown in Figure 6. It shows the standard deviation of the comparator is around 3mV.

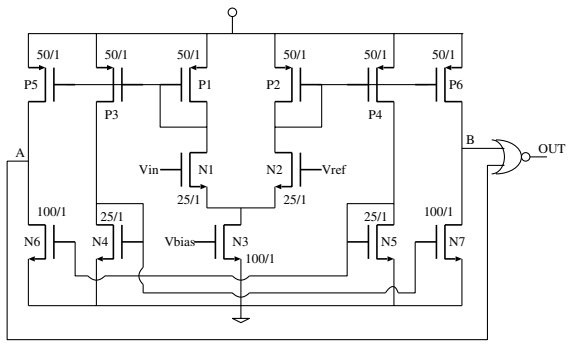

Figure 6. OTA-based window comparator.

4.2 Inverter-based comparators

By exploiting the fact that inverter threshold can be adjusted through changing device size ratios, inverter circuits have been used as analog comparators [10] or even quantizers in analog-to-digital converter design [4]. Such circuits have small footprints and do not require reference signals, but suffer the drawback of large threshold variations. In the PCA testing circuits, this drawback can be partially compensated by increasing integration cycles.

A straightforward implementation of inverter-based window comparators is shown in Figure 7(a). It contains two inverters with different threshold voltages (denoted as V_H and V_L; $V_H > V_L$). If its analog input is within the range from V_L to V_H, the comparator output is logic **1**; else it is **0**. To use this type of comparators the integration cycles must be selected relatively large, implying that comparators must have large thresholds. If signal ground level is $\frac{V_{DD}}{2}$, thresholds of the comparator shown in Figure 7(a) are $\frac{V_{DD}}{2} - V_L$ and $V_H - \frac{V_{DD}}{2}$. Theoretically, the maximum and minimum inverter thresholds are $V_{DD} - |V_{tp}|$ and V_{tn}, respectively. Therefore, the maximum achievable window comparator threshold is either $\frac{V_{DD}}{2} - V_{tn}$ or $\frac{V_{DD}}{2} - |V_{tp}|$.

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With low power supply, the maximum comparator threshold of the straightforward design may not be large enough. Hence, level shifters can be used to shift the analog input before it is digitized by inverters as shown in Figure 7(b) and (c). Note that the inverter-nor gate is omitted in Figure 7(b) and (c) for the reason of conciseness. The level shifters are implemented using PMOS or NMOS source followers depending on the desired shifting directions. The use of level shifters helps avoid inverters whose thresholds are close to their theoretical limitations: $V_{DD} - |V_{tp}|$ or V_{tn}. Such inverters normally require large device sizes and, hence, are preferred to be avoided.

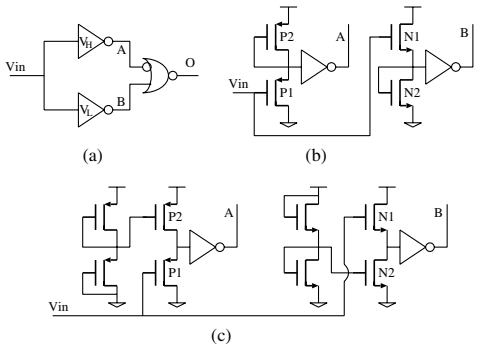

Figure 7. Inverter-based window comparators.

The impact on comparator threshold variations caused by adding level shifters has to be carefully treated in the design process. For level shifters in Figure 7(b), their small signal gains can be derived as:

$$G = \frac{1}{1 + \sqrt{\frac{(W/L)_2}{(W/L)_1}}} \tag{12}$$

where $(W/L)_1$ and $(W/L)_2$ are transistor sizes of N_1 and N_2 for the NMOS level shifter, or P_1 and P_2 for the PMOS level shifter. Since the input-referred threshold deviation is inversely proportional to the small signal gain of the level shifter, G is preferred to be as close to 1 as possible. This implies that the ratio of $\frac{(W/L)_2}{(W/L)_1}$ should be selected small in the design process. This observation is confirmed by simulation results, which are represented by the two dot lines in Figure 8. In the legends of the figure, *P-INV* and *N-INV* stand for inverters with PMOS and NMOS level shifters, respectively.

For level shifters in Figure 7(c), their small signal gains are determined by the transconductance of the driving devices (N_1 or P_1) and output resistance of both driving and load transistors in the level shifter. Changing the ratio of $(W/L)_1$ over $(W/L)_2$ has little impacts on their small signal gains. In this scenario, devices N_1 and N_2 (as well as P_1 and P_2) should have the same size in order to minimize mismatches between N_1 and N_2. As shown in Figure 8, the comparator in Figure 7(c) exhibits the smallest threshold deviation when $(W/L)_1 = (W/L)_2$. From the given simulation data, the comparator in Figure 7(c) always has smaller variations than the circuit given in Figure 7(b). This fact is partially due to the process variation and device mismatch profile used in our simulation. It may vary with different fabrication processes.

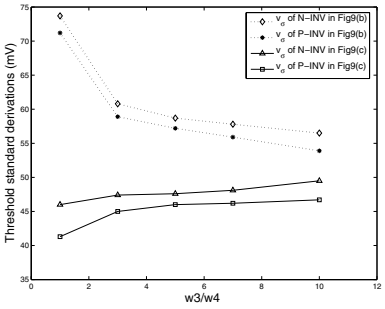

Figure 8. Threshold variations of inverter-based window comparators.

5. Experimental results

Circuit simulations are performed to investigate the performance of the two comparators in PCA testing operations. To demonstrate the validity of the proposed BIST techniques, circuit simulations are performed to detect PCA faults using the proposed testing method. Each PCA contains 8 binary-weighted capacitors and its value can be programmed from 1 to 255 unit capacitance, which is 400fF. CAB switches are implemented using CMOS transmission gates. The sizes of PMOS and NMOS transistors in the transmission gate are selected to be the same (10μ/0.4μ) in order to minimize channel charge injection and clock feedthrough. The clock frequency used in the experiment is 1MHz, and the power supply is 3.3V. To reduce simulation time, an op-amp macromodel is used in simulation. Its key performance parameters are summarized as follows: *Low frequency gain = 74dB, Unit-gain frequency = 10MHz, Common mode rejection ratio = 70dB, Input offset voltage = 4mV, Slew Rate = 20V/μs, Settling time (0.1%) = 0.5μs, Power supply = 3.3V and Output swing range =* $0.18V \sim 3.1V$

Two other parameters which need to be determined in the experimental setup are, the value of feedback capacitor C_f and the number of integration cycles. We propose two approaches for this purpose. The first method, called *comparator-oriented approach*, starts from the threshold of the analog window comparator. It is preferred when the

selection of comparator threshold is restricted and the comparator circuit exhibits small threshold variations. Assume that the threshold and its standard deviation of the comparator are V_ϵ and v_σ, respectively. For each testing configuration, the values of C_f and k should be selected such that after k integration cycles the integrator output reaches a level which is very close to, but does not exceed, $V_\epsilon - 3 \cdot v_\sigma$. Since C_f has discrete values, a computer program can be used to search the combination of C_f and k that leads to the integrator output coming close to $V_\epsilon - 3 \cdot v_\sigma$ the most. When multiple such combinations exist, the one with the smallest k value is preferred. The second method, referred to as *maximum-threshold approach*, is suitable for BIST circuits using inverter-based window comparators. In such circuits, the thresholds of comparators are desired to be as large as possible. The large comparator threshold will allow more integration cycles, which consequently leads to more effective diminution of the negative impact of comparator threshold variations. Assume the maximum output of the op-amp while it maintains its linearity is V_{amp}^{max}. This value is also the maximum output of the integrator circuit before it starting to lose its linearity. From the discussion in Section 3, we can conclude that the comparator threshold should be selected as $V_{amp}^{max} - 3 \cdot v_\sigma$. In addition, the maximum allowed integrator output in fault-free scenarios should not exceed $V_{amp}^{max} - 6 \cdot v_\sigma$. Therefore, this criterion can be used to select the combination of C_f and k for the BIST circuit configuration.

The above approaches have been applied with the OTA-based and inverter(INV)-based comparators, respectively. Table 1 gives the ranges of parametric faults detected by the two comparators. While Table 2 shows the number of integration cycles required for the detection of arbitrarily selected parametric faults. Clearly the INV-based comparator requires more number of to produce the same results as the OTA-based comparator.

Table 1. Ranges of detectable faults.

	Ranges of detectable faults	
Parametric Faults	OTA-based	INV-based
Leakage (R_{leak})	$0 \sim 770K\Omega$	$0 \sim 430.5K\Omega$
Bridge (R_b)	$0 \sim 175M\Omega$	$0 \sim 12.25M\Omega$
Large on-resist.(R_{on})	$200K\Omega \sim \infty$	$302K\Omega \sim \infty$
Small off-resist.(R_{off})	$0 \sim 275M\Omega$	$0 \sim 7M\Omega$

6. Concluding remarks

In this work, we studied the problem of how window comparator threshold variations affecting the efficiency of PCA BIST circuits. Principles obtained in this study can be potentially applied to other analog BIST circuits that contain window comparators. To address the issue of comparator threshold variations in PCA testing, two window comparator circuits are developed. The first comparator has a fully symmetric structure which results in small threshold variations. This design also has several other advantages, making it suitable for a wide range of testing applications. The second design is based on digital inverter circuits, which has a very small footprint. It relies on increasing testing time to reduce the effects of its large threshold deviations. Circuit simulations are conducted to investigate the performance of PCA BIST circuits with using the above two design approaches. Experimental results provide a useful comparison that may help the selection of proper design approaches in the development of PCA testing circuits.

Table 2. Comparison of integration cycles.

Integration cycles required for detecting specific faults		
Specific fault values	OTA-based	INV-based
$R_{leak} = 300K\Omega$	5	21
$R_b = 5M\Omega$	2	7
$R_{on} = 500K\Omega$	3	6
$R_{off} = 5M\Omega$	2	9

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