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Investigating the Efficiency of Integrator-Based Capacitor Array Testing Techniques

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Investigating the Efficiency of Integrator-Based Capacitor Array Testing Techniques

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Abstract

This paper presents techniques to model the impact of parametric faults on the performance of programmable capacitor arrays (PCAs). Closed-form equations are derived for estimating ranges of parametric faults that can be detected by integrator-based PCA testing circuits. Methods to improve PCA testing efficiency are discussed and experimental results are reported.

1 Introduction

With the increasing use of Field Programmable Analog Arrays (FPAAs) in electronic design, testing of FPAA circuits has attracted significant research interests from the testing community. Research work has been reported on testing circuits implemented on FPAAs [10, 16, 4, 8, 11, 13, 14, 3, 12]. Efforts have also been devoted to systematically testing hardware resources on FPAA platforms [1, 6]. Among various reconfigurable components, programmable capacitor arrays (PCAs) are important building blocks in switched-capacitor (SC) based FPAAs and, hence, should be thoroughly tested. Previously, SC-integrator based built-in-self-testing (BIST) techniques were proposed in [2] for testing PCAs on FPAA platforms. In this work, we investigate the efficiency of the integrator-based PCA BIST circuits in single-fault scenarios. Closed-form equations are derived for estimating the ranges of parametric faults that can be detected. Techniques to improve PCA testing efficiency are also discussed.

The rest of the paper is organized as follows. Section 2 explains preliminaries of this work. Section 3 develops techniques to estimate detectable ranges of PCA parametric faults. Methods to improve the efficiency of PCA BIST circuits are discussed in Section 4. Experimental results are provided in Section 5 and the paper is concluded in Section 6.

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2 Preliminaries

2.1 PCA fault models

A PCA normally contains a set of binary-weighted capacitor branches connected in parallel. For each capacitor branch, a serial switch is used to configure the connection between this branch and the rest of the capacitors. To achieve good capacitor matching, all PCA binary-weighted capacitor branches are made of equally-sized small capacitors, which are referred to as unit capacitors.

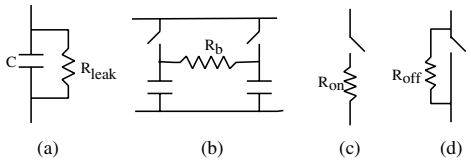

Figure 1. PCA parametric faults.

Various parametric faults may occur in a PCA. A unit capacitor may not have the correct value. This is called unit capacitor fault. Leakage paths may exist in the isolation layer between the two terminals of a unit capacitor, leading to a leakage fault whose fault model is given in Figure 1(a). Due to dust or excess metal, two interconnects ideally isolated may become connected through a resistive path. This is called bridge fault and its fault model is shown in Figure 1(b). Switches used in PCAs are normally implemented using transmission gates. Their switching characteristics can be deteriorated by excessively large on-resistance or excessively small off-resistance [7]. These two types of faults are referred to as large on-resistance fault ($\mathcal{R}_{on}$ fault) and small off-resistance fault ($\mathcal{R}_{off}$ fault), as modeled in Figure 1(c) and (d), respectively. Note that only a subset of parametric faults associated with switches are discussed in the above description. Other parametric faults such as *Gate Oxide Short* (GOS) faults, are not included because they can be detected by other testing methods such as IDDQ testing [9].

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2.2 Integrator-based PCA testing techniques

A previously proposed integrator-based PCA BIST circuit [2] is depicted in Figure 2. Assuming $C_A = C_B$ and both fault-free, the output of the integrator should be ideally at the signal ground level as the net charge transferred from both C_A and C_B to C_f is zero during each integration cycle. Otherwise net charge will be accumulated at capacitor C_f, resulting in the integrator output to deviate from the signal ground level. During the testing process, the integrator output is fed to a window comparator after a fixed number of integration cycles. If the difference between the signal ground and the integrator output is within the range of $[-V_\epsilon, V_\epsilon]$, where V_ϵ is referred to as the window comparator *threshold*, the comparator output is logic **1** to indicate that the circuit is fault-free. Otherwise, the comparator output is logic **0** marking the occurrence of faults.

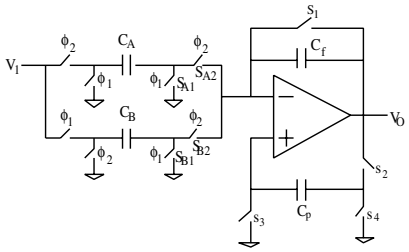

Figure 2. Integrator-based PCA BIST circuit.

The integrator output normally does not remain at the signal ground level even in fault-free cases, due to capacitor mismatches, channel charge injection, clock feedthrough, and not fully canceled input offset voltage of the operational amplifier (op-amp). We use V_k^{max} to denote the largest possible integrator output after k integration cycles in fault-free scenarios. The value of V_k^{max} can be estimated through circuit analysis or by performing Monte Carlo or corner simulations. Typically, the window comparator threshold V_ϵ is selected to be slightly larger than V_k^{max} [5, 15]. Also, a fault is more difficult to be detected if the fault and circuit parasitics cause opposite effects on the integrator output. In this case, a fault can be detected only if the total charge that is transferred to C_f by the fault effect is greater than $C_f \cdot (V_\epsilon + V_k^{max})$.

3 Estimating Detectable Parametric Faults

Among the five PCA parametric faults discussed in Section 2.1, unit capacitor faults can be directly converted to capacitance difference between the integrator input branches. Consequently, the detectable range of unit capacitor faults can be easily estimated. In this section, we develop techniques to estimate detectable ranges of the other parametric faults.

3.1 Ranges of detectable $\mathcal{R}_{on}$ faults

An $\mathcal{R}_{on}$ fault increases the circuit RC delay and, consequently, prevents the capacitor from being fully charged (or discharged) during the corresponding clock phase. As a result, there will be less charge transferred from the faulty input branch to the integrator feedback capacitor. The same effect can be achieved by eliminating the large on-resistance and reducing the capacitor value. Therefore, an $\mathcal{R}_{on}$ fault can be modeled by a fault-free circuit with an attenuated capacitor as shown in Figure 3. The *attenuation factor* α,

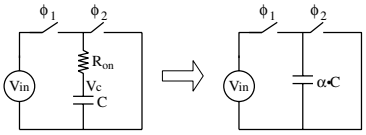

Figure 3. Modeling $\mathcal{R}_{on}$ faults by capacitor attenuation.

which is the ratio of the reduced capacitor value to its original value, is derived as follows. We use V_c^k to denote the voltage across Capacitor C after ϕ_1 phase of the kth clock cycle. Then, we have the relation:

$$V_c^k = V_{in} \cdot (1 - \mu) + V_c^{k-1} \cdot \mu^2 \tag{1}$$

where $\mu = e^{\frac{-T}{2 \cdot R_{on} \cdot C}}$ and T is the period of the clock used in the circuit. This recursive equation can be re-written as:

$$V_c^k = V_{in} \cdot (1 - \mu) \cdot \frac{1 - \mu^{2 \cdot (k+1)}}{1 - \mu^2} + V_c^0 \cdot \mu^{2 \cdot k} \tag{2}$$

where V_c^0 is the initial voltage across Capacitor C. When the value of $R_{on} \cdot C$ is much less than $\frac{T}{2}$, μ is very small. Consequently, the above equation can be approximated as:

$$V_c^k = V_{in} \cdot (1 - \mu) \tag{3}$$

During the kth clock cycle charge transferred by Capacitor C can be calculated as:

$$Q = C \cdot V_c^k \cdot (1 - \mu) = C \cdot V_{in} \cdot (1 - \mu)^2$$

Hence, the capacitor attenuation factor is:

$$\alpha = (1 - \mu)^2 \tag{4}$$

Figure 4 compares the amounts of transferred charge that are obtained from circuit simulation and estimation using α. Note that the on-resistance values shown in the figure are normalized by the maximum allowed on-resistance value R_{max}, which is defined as the resistance that guarantees at the end of a charging cycle the voltage across the capacitor

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reaching 99.9% of its ideal value. The relative error between estimation and simulation is also shown in the figure. It indicates that the capacitor attenuation model is quite accurate when $R_{on} < 4.5 \cdot R_{max}$. As shown in later sections, the minimum detectable $\mathcal{R}_{on}$ faults normally have values smaller than $4 \cdot R_{max}$. Therefore, the capacitor attenuation model works well for estimating detectable ranges of $\mathcal{R}_{on}$ faults.

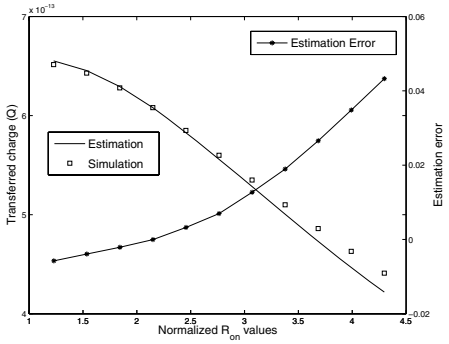

Figure 4. Comparison of predicted and simulated charge transfer.

Without losing generalities, we assume an $\mathcal{R}_{on}$ fault occurs at PCA C_A in Figure 2. As a result, the net charge transferred to C_f due to the $\mathcal{R}_{on}$ fault is:

$$\Delta Q = \alpha \cdot C_A \cdot V_{in} - C_B \cdot V_{in} \tag{5}$$

According to the previous discussion, the condition to detect this fault after k integration cycles is:

$$k \cdot \Delta Q \geq C_f \cdot (V_\epsilon + V_k^{max}) \tag{6}$$

From this inequality, the range of detectable $\mathcal{R}_{on}$ faults can be solved as:

$$R_{on} \geq \frac{-T}{2 \cdot C_A} \cdot \frac{1}{\ln(1 - \sqrt{\alpha_{min}})} \tag{7}$$

where α_{min} is:

$$\alpha_{min} = 1 - \frac{(V_\epsilon + V_k^{max})}{k \cdot V_{in}} \cdot \frac{C_f}{C_B} \tag{8}$$

3.2 Ranges of detectable $\mathcal{R}_{off}$ and bridge faults

Although $\mathcal{R}_{off}$ and bridge faults are due to different mechanisms, they affect the integrator circuit in a similar manner. Hence, we can develop a single method to predict the detectable ranges of $\mathcal{R}_{off}$ or bridge faults. Due to an $\mathcal{R}_{off}$ or bridge fault, an extra RC network, consisting of R_x and C_x, will participate in charge transfer during integration operations as shown in Figure 5. As described early, the voltage across capacitor C_x can be calculated using Equation 2. The most difficult detectable $\mathcal{R}_{off}$ or bridge fault results in large R_x value, and its corresponding μ value is close to 1. Therefore, in this case Equation 2 can be simplified as:

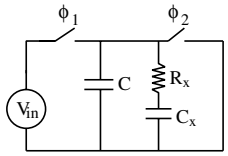

Figure 5. Effect of $\mathcal{R}_{off}$ faults or bridge faults

$$V_c^k = V_c^0 \cdot \mu^{2 \cdot k} \tag{9}$$

After k integration cycles, extra charge Q_k transferred by the $R_x C_x$ network, introduced by either an $\mathcal{R}_{off}$ or bridge fault, can be calculated as:

$$Q_k = V_c^0 C_x \frac{1 - \mu^{2(k+1)}}{1 - \mu^2}(1 - \mu) \approx V_{in} C_x \frac{1 - \mu^{2(k+1)}}{2} \tag{10}$$

In the above derivation, we assume $V_c^0 = V_{in}$ and use the approximation of $\mu \approx 1$.

A more accurate approximation of Equation 2 is:

$$V_c^k = \frac{1}{2} \cdot V_{in} \cdot (1 - \mu^{2 \cdot (k+1)}) + V_c^0 \cdot \mu^{2 \cdot k} \tag{11}$$

From this equation, Q_k can be estimated as:

$$\begin{aligned} Q_k &= \frac{1}{2} k (1 - \mu) C_x V_{in} - \frac{1}{4}(1 - \mu^{2 \cdot (k+1)}) C_x V_{in} \\ &+ \frac{1}{2}(1 - \mu^{2 \cdot (k+1)}) C_x V_c^0 \end{aligned} \tag{12}$$

Assuming $V_c^0 = V_{in}$, the above equation can be simplified as:

$$Q_k = \frac{1}{2} k (1 - \mu) C_x V_{in} + \frac{1}{4}(1 - \mu^{2(k+1)}) C_x V_{in} \tag{13}$$

For the convenience of discussion, we refer to Q_k estimation methods described by Equations 10 and 13 as *Model 1* and *Model 2*, respectively. Figure 6 compares estimated charge with circuit simulation results. Two R_x values, which are given in terms of R_{min} in the figure, are used in the comparison. R_{min} is the minimum required resistance that can practically isolate C_x from Capacitor C. Its value is selected such that the charge transferred by the $R_x C_x$ network during one clock cycle is less that 0.1% of $C_x \cdot V_{in}$. The comparison shows that both models are accurate when R_x value is close to R_{min} (e.g. $R_x = 0.5 \cdot R_{min}$). When R_x value is significantly smaller than R_{min} (e.g. $R_x = 0.1 \cdot R_{min}$). Model 1 loses its accuracy quickly with the increase of integration cycles. However, Model 2 keeps its accuracy intact.

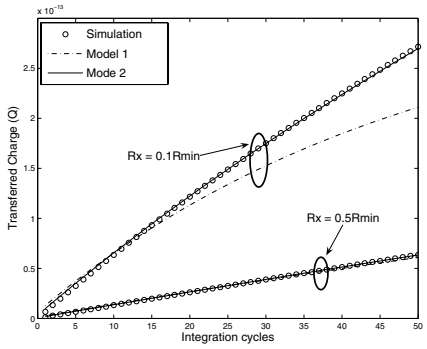

Figure 6. Comparison of charge from simulation and estimation.

The condition for an $\mathcal{R}_{off}$ or bridge fault to be detected is: $Q_k \geq C_f \cdot (V_\epsilon + V_k^{max})$. As the first attempt, Model 1 can be used with the above condition to find the detectable ranges of $\mathcal{R}_{off}$ or bridge faults as:

$$R_x \leq \frac{-T \cdot (k+1)}{C_x \cdot \ln(1 - 2 \cdot \frac{C_f \cdot (V_\epsilon + V_k^{max})}{C_x \cdot V_{in}})} \tag{14}$$

If the obtained R_x is significantly smaller than R_{min}, it indicates that the estimation result may not be accurate. Then, Model 2 has to be used for a more accurate estimation. In this approach, the value of μ, denoted as μ_c, that makes $Q_k = C_f \cdot (V_\epsilon + V_k^{max})$ can be obtained by solving the following equation:

$$\mu_c^{2 \cdot (k+1)} + 2 \cdot k \cdot \mu_c - b = 0 \tag{15}$$

where b is:

$$b = 2 \cdot k + 1 - \frac{4 \cdot C_f}{C_x} \cdot \frac{V_\epsilon + V_k^{max}}{V_{in}} \tag{16}$$

Various mathematical packages can be used to numerically find μ_c solutions. In practical cases, b is always positive, which guarantees that Equation 15 has at least one positive real root. Once μ_c is obtained, the maximum detectable $\mathcal{R}_{off}$ or bridge fault can be estimated as:

$$R_x^{max} = -\frac{T}{2 \cdot C_x \cdot \ln \mu_c} \tag{17}$$

3.3 Ranges of detectable leakage faults

The leakage fault in PCA C_A will result in a DC path from the integrator input to the virtual ground node during ϕ_2 phase as shown in Figure 7. Since difficult detectable leakage faults are normally associated with PCA branches with large capacitor values, the on-resistance of switches in the capacitor charging path has to be considered for a more accurate estimation. In the following discussion, we use R_{sw} to denote the total on-resistance of switches. During

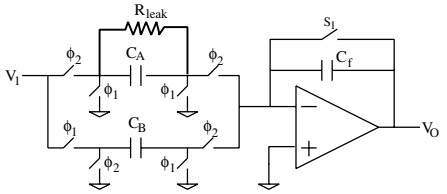

Figure 7. Modeling PCA leakage faults.

clock ϕ_2 phase, the voltage across C_A as well as R_{leak} is described as:

$$V_{C_A}(t) = V_{in} \cdot (1 - e^{\frac{-t}{R_{sw} \cdot C_A}}) \tag{18}$$

Hence, the charge transferred to C_f by R_{leak} during one clock cycle is:

$$Q_l = \int_0^{\frac{T}{2}} \frac{V_{C_A}(t)}{R_{leak}} \cdot dt \approx \frac{V_{in}}{R_{leak}} \cdot (\frac{T}{2} - R_{sw} \cdot C_A)$$

Similarly, the condition for detecting the leakage fault after k clock cycles is: $k \cdot Q_l \geq C_f \cdot (V_\epsilon + V_k^{max})$. Therefore, we can find the range of detectable leakage faults as:

$$R_{leak} \leq \frac{V_{in}}{V_\epsilon + V_k^{max}} \cdot \frac{\frac{T}{2} - R_{sw} \cdot C_A}{C_f} \cdot k \tag{19}$$

4 Techniques to Improve Testing Efficiency

4.1 Reducing the impact of comparator threshold variations

The window comparator threshold is selected slightly larger than the fault-free integrator output in order to prevent testing circuits from labeling good devices as faulty due to measurement inaccuracy. Since the testing circuits do not involve off-chip connections, the measurement inaccuracy is mainly dominated by window comparator threshold variations, which are often described by a *mean value* $\bar{V_\epsilon}$ and a *standard deviation* v_σ. A sound design approach is to select $\bar{V_\epsilon}$ larger than V_k^{max} by $3 \cdot v_\sigma$. Assuming that the variation of the comparator threshold follows Gaussian distribution, this approach guarantees that the possibility to label a good device *faulty* is smaller than 0.3%. It is also easy to see that 99.7% of all the comparators have threshold in the range $[\bar{V_\epsilon} - 3 \cdot v_\sigma, \bar{V_\epsilon} + 3 \cdot v_\sigma]$. Therefore, $\bar{V_\epsilon} + 3 \cdot v_\sigma$ can be practically treated as the comparator threshold in the worst case.

Substituting $V_\epsilon = \bar{V_\epsilon} + 3 \cdot v_\sigma$ into Equations 7 and 8, the minimum detectable $\mathcal{R}_{on}$ faults can be estimated. Assuming $C_A = C_B = 20pF$ and $C_f = 8pF$, the estimated detectable fault values are plotted in Figure 8. Three comparator threshold standard deviations, $v_\sigma = 10mv$, $20mv$, and $40mv$, are selected in the study and their corresponding detectable faults are plotted using solid, dot, and dash

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lines, respectively. It is not a surprise to see that the fault detection capability is degraded when v_σ is large. The plot also reveals that increasing integration cycles can partially overcome the negative impact caused by large v_σ. For example, to detect a large on-resistance fault that has the value of $1.2 \cdot R_{max}$, if comparator v_σ is 10mV, only 4 integration cycles are needed in the testing process. However, if the comparator v_σ is 40mV, 14 integration cycles have to be performed to achieve the same level of fault detection capability. With the increase of integration cycles, comparator thresholds, indicated by solid lines with legends in Figure 8, have to be increased accordingly. Although this case study is based on $\mathcal{R}_{on}$ faults, the conclusion is applicable to other parametric faults

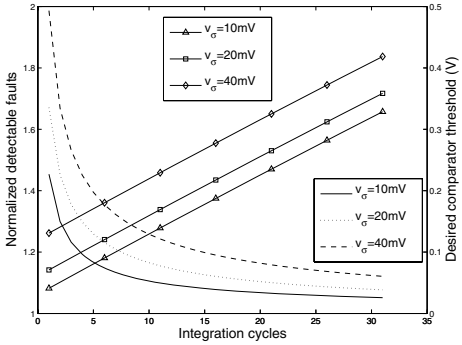

Figure 8. Detectable $\mathcal{R}_{on}$ vs. integration cycles

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4.2 Setting proper circuit initial conditions

The discussion in Section 3.2 indicates that charge transferred by the R_xC_x network (resulted from an $\mathcal{R}_{off}$ or bridge fault) depends on the initial voltage V_c^0 across capacitor C_x. Figure 9 compares charge transferred by the R_xC_x network with circuit initial conditions of $V_c^0 = 0$ and $V_c^0 = V_{in}$. It shows that there is significantly more charge transferred by the R_xC_x network when $V_c^0 = V_{in}$. As a result, larger ranges of $\mathcal{R}_{off}$ and bridge faults can be detected if testing operations start with the initial circuit condition of $V_c^0 = V_{in}$. To set up the proper initial condition for PCA BIST circuits, a set of selected switches can be kept close for a time period that is approximately $R_{min} \cdot C_x$ to allow Capacitor C_x be fully charged before starting integration operations. This can be easily achieved with the help of simple clock gating circuits.

5 Experimental Results

Circuit simulations are conducted to investigate the efficiency of PCA testing circuits. In our simulation setup, each PCA contains 8 binary-weighted capacitors and its value can be programmed from 1 to 255 unit capacitance, which is

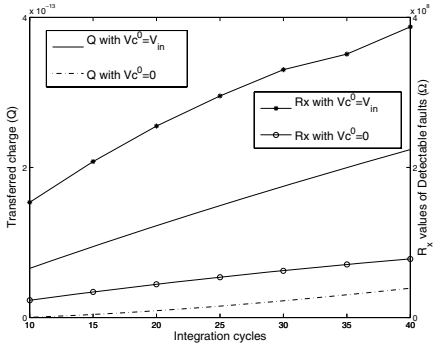
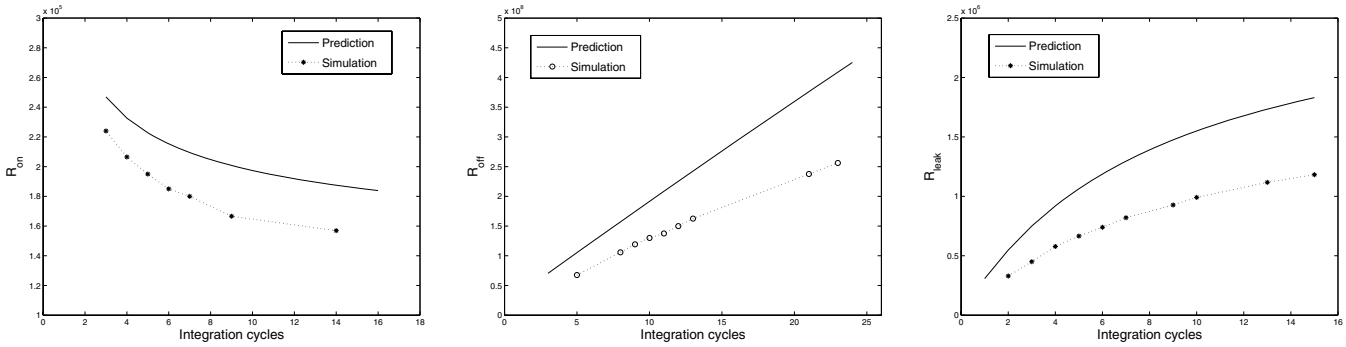


Figure 9. Detectable $\mathcal{R}_{off}$ faults vs. different circuit initial condition.

400fF. CAB switches are implemented using CMOS transmission gates. The sizes of PMOS and NMOS transistors in the transmission gate are selected to be the same (10μ/0.4μ) in order to minimize channel charge injection and clock feedthrough. The clock frequency used in the experiment is 1MHz, and the power supply is 3.3V. To reduce simulation time, an op-amp macromodel [2] is used in simulation.

The minimum detectable $\mathcal{R}_{on}$ faults and maximum detectable $\mathcal{R}_{off}$ and leakage faults obtained from circuit simulation and estimation are compared in Figure 10. Because $\mathcal{R}_{off}$ and bridge faults share the same estimation model, comparison between simulated and estimated bridge faults are not included in the paper for the reason of conciseness. It shows that the developed estimation techniques can reasonably predict the ranges of detectable parametric faults when the numbers of integration cycles are small. The difference between estimation and simulation results increases when the number of integration cycles is rising. This is due to the accumulated circuit parasitic effects, including channel charge injection, clock feedthrough, and op-amp settling time. It is observed that simulation results become closer to estimation values with increasing op-amp gain and decreasing settling time. Also, reported in Figure 10 are faults occurred at positions that make the faults most difficult to be detected (e.g. $\mathcal{R}_{on}$ and $\mathcal{R}_{off}$ faults in 1C branch, leakage fault in 128C branch). For faults occurring at other positions, smaller difference between simulation and estimation results are observed. Future efforts will be directed toward the investigation of techniques that minimize circuit parasitic effects in the estimation of detectable PCA parametric faults. Here we have considered only single fault scenarios. Although fault cancellation happens in multiple-fault scenarios, the existence of multiple fault often makes it easy to detect PCA faults when using the integrator-based PCA BIST circuits. Thus, the predicted capability for detecting single faults is a reasonable metric to measure the efficiency of the PCA BIST circuits.

Table 1 compares the required number of integration cy-



(a) $\mathcal{R}_{on}$ faults (b) $\mathcal{R}_{off}$ faults (c) Leakage faults

Figure 10. Comparing detectable parametric faults from simulation and estimation.

cles that guarantee the probability of detecting the given faults is higher than 0.997 in the occurrence of comparator threshold variations with $V_\epsilon = 200m$V. It shows PCA BIST circuits using window comparators that have large threshold deviations require longer testing time in order to achieve the same level of fault detection capability as BIST circuits which use comparators with small v_σ. This is consistent with the analysis in Section 4.1. Table 2 lists the maximum detectable $\mathcal{R}_{off}$ and bridge faults when the testing operations start with different circuit initial conditions. The reported faults are detected within 20 integration cycles. The results clearly support the conclusion drawn in Section 4.2.

Table 1. Required integration cycles

Parametric faults	Threshold standard deviation		
	$5mV$	$15mV$	$30mV$
$R_{on} = 170K\Omega$	18	20	24
$R_{off} = 110M\Omega$	20	23	27
$R_{bridge} = 95M\Omega$	18	20	25
$R_{leak} = 1M\Omega$	22	26	29

Table 2. Detectable $\mathcal{R}_{off}$ and bridge faults.

Parametric faults	Circuit initial conditions	
	$V_c^0 = V_{in}$	$V_c^0 = 0$
R_{off}	$270M\Omega$	$35M\Omega$
R_{bridge}	$220M\Omega$	$21.5M\Omega$

6 Concluding Remarks

In this work, circuit models are developed to study the impact of PCA parametric faults on SC integrator circuits. These models can be potentially extended to model parametric fault effects in general SC circuits. Based on the developed circuit models, closed-form equations are derived for estimating the ranges of detectable PCA parametric faults. Also, techniques to improve the efficiency of integrator-based PCA testing circuits are presented.

References

[1] A. Andrade, G. Vieira, and e. M. Lubaszewski. Testing global interconnects of field programmable analog arrays. In *Proc. 10th International Mixed-Signal Testing Workshop*, pages 231–246, 2004.

[2] A. Laknaur and H. Wang. Built-in-self-tesiting techniques for programmable capacitor arrays. In *Proc. ISQED*, pages 434–439, 2005.

[3] A. Laknaur and H. Wang. A methodology to perform online self-testing for field programmable analog circuits. *IEEE Trans. Instrimentation and Measurement*, 54(5):1751–1760, 2005.

[4] C. A. Looby and C. Lyden. Field programmable analogue arrays: A dft view. In *IEE Colloquium on Testing Mixed Signal Circuits and Systesm*, 1997.

[5] P. Mullenix. The capability of capability indics with an application to guardbanding in a test environment. In *Proc. International Test Conference*, pages 907–915, 1990.

[6] G. Pereria, M. Lubaszewski, A. A. Jr, T. Balen, F. Azias, and M. Renovell. Testing the interconnect networks and i/o resources of field programmable analog arrays. In *Proc. VLSI Test Symposium*, pages 389–394, 2005.

[7] e. a. R. Rodriguez-Montanes. Analog switches in programmable analog devices: Quiescent defective behaviours. In *IEEE International On-Line Testing Workshop*, 2002.

[8] R. Sanahuja, V. Barcons, L. Balado, and J. Figueras. Testing biquad filters under parametric shifts using x-y zoning. In *Proc. Intl Mixed-Signal Test Workshop*, 2003.

[9] J. Segura, C. D. Benito, A. Rubio, and C. F. Hawkins. A detailed analysis of gos defects in mos transistors: testing implications at circuit level. In *Proc. ITC*, pages 544–551, 1995.

[10] T. Slaughter and C. Stroud. Fault injection emulation for field programmable analog arrays. In *Proc. Southwest Symp. Mixed-Signal Design*, pages 212–216, 2003.

[11] T.Balen, A. Jr, F.Azais, M.Lubaszewski, and M. Renovell. An approach to the built-in self-test of field programmable analog arrays. In *Proceeding of IEEE VLSI Test Symposium*, 2004.

[12] T.Balen, A. Jr, F.Azais, M.Lubaszewski, and M. Renovell. Testing the configurable analog blocks of field programmable analog arrays. In *Proc. International Test Conference*, pages 893–902, 2004.

[13] H. Wang, S. Kulkarni, and S. Tragoudas. Circuit techniuqes for field programmable analog array on-line testing. In *Proc. 10th International Mixed-Signal Testing Workshop*, pages 237–244, 2004.

[14] H. Wang, S. Kulkarni, and S. Tragoudas. Online testing field programmable analog array circuits. In *Proc. 10th International Test Conference*, pages 1340–1348, 2004.

[15] R. H. Williams and C. F. Hawkins. The economics of guardband placement. In *Proc. ITC*, pages 218–225, 1993.

[16] R. S. Zebulum and e. a. D. Keymeulen. Experimental results in evolutionary fault-recovery for field programmable analog devices. In *Proc. NASA/DoD Conf. on Evolvable Hardware*, 2003.