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On-line Testing Field Programmable Analog Array Circuits

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Abstract

This paper presents an efficient methodology to on-line test field programmable analog array (FPAA) circuits. It proposes to partition the FPAA circuit under test into sub circuits. Each sub circuit is tested by replicating the sub circuit with programmable resources on FPAAs, and comparing the outputs of the the original partitioned sub circuit and its replicaton. The advantages of this approach includes: low implementation cost, enhanced testability, and flexible testing schedules. This paper also presents circuit techniques to address stability problems which are often encountered in the proposed on-line testing approach. In addition, the impact of performing circuit partition on testability is investigated in this work. It shows that testability is generally improved in partitioned circuits. Finally, experimental results are presented to demonstrate the feasibility and effectiveness of the proposed techniques.

1 Introduction

Field programmable analog arrays (FPAAs) are the counterparts of field programmable gate arrays (FPGAs) in analog domain. In the past few years, numerous efforts have been devoted to developing FPAA technologies [1, 2, 3]. At present, quite a few commercial FPAA products [4, 5, 6] are already on the market. Such devices have been used to implement signal conditioning, filtering, data acquisition, closed-loop control, and other analog functions for a wide range of applications. Since many of these FPAA applications involve high reliability requirements, techniques to effectively test FPAA circuits are becoming increasingly important. Very recently, several techniques for FPAA testing have been developed [7, 8, 9, 10]. Also, it has been proposed to exploit the programmability of FPAAs in the implementation of fault-recovery systems for space applications [11]. In this paper, we investigate techniques to perform on-line testing for FPAA circuits. The proposed methodology not only provides an on-line testing solution but also locates faulty circuit blocks. Therefore, this methodology is highly desirable in applications where FPAAs are used to implement fault-recovery systems.

Although various techniques have been developed for on-line testing digital systems, methods to perform analog on-line testing are still limited. Current analog on-line testing techniques can be mainly classified into *redundancy-based* and *non-redundancy-based* approaches. The redundancy-based approach duplicates the entire or a portion of the circuit under test (CUT), and compares the outputs of the original circuit and its replication [12, 13, 14]. The non-redundancy-based approach relies on Built-In-Self-Test (BIST) circuits to measure certain performance metrics of the CUT. This approach includes concurrently monitoring current consumption [15], statistical properties [16], common mode signals at fully differential circuits [17, 18], and other types of circuit signals [19, 20, 21, 22, 23]. By taking advantage of special properties of circuits under test, the non-redundancy-based approach normally requires small hardware overhead. However, this approach may not be able to achieve high fault coverage for certain types of circuits, and sometimes involve testing circuits that are difficult to design. On the contrary, the redundancy-based approach usually requires significant hardware cost. But it is easy to implement and has the potential to achieve high fault coverage. More interestingly, this approach can be used to locate malfunctioning circuit blocks.

To reduce hardware cost in the redundancy-based approach, programmable Biquad modules have been used to perform on-line testing for filter circuits that consist of cascaded Biquad filters [12, 14]. By exploiting the regularity of Biquad filters, a programmable Biquad module is periodically programmed to duplicate different Biquads of the filter circuits. In this paper, we present a methodology to use programmable analog circuits to perform on-line testing for general active linear circuits. The proposed approach partitions the CUT into smaller circuit blocks than Biquad structures. This results in lower implementation cost and enhanced circuit testability. In addition, we developed new techniques to address circuit stability problems, which are often encountered when only a portion of the CUT is duplicated to perform redundancy-based on-line testing. Although a similar problem has also been addressed in [13], our solution is more cost-effective and

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easy to implement. Finally, this paper investigates the impact of performing circuit partition on testability. Conclusions drawn from this study provide useful guidance on efficiently implementing the proposed on-line testing methodology.

The rest of the paper is organized as follows. Section 2 introduces the preliminaries of this work. We first explain FPAA technologies in Section 2.1. Then, the concept of the proposed FPAA on-line testing methodology is described in Section 2.2. The advantages and potential applications of the proposed method are also discussed in this section. The developed circuit techniques are presented in Section 3. Section 4 studies how testability is affected by performing circuit partition. Experimental results are provided in Section 5, and the paper is concluded in Section 6.

2 Preliminaries

2.1 Field Programmable Analog Array Technologies

An FPAA device normally contains Configurable Analog Blocks (CABs), Interconnect networks, I/O circuits, and on-chip memories. CABs consist of primitive analog components whose values and connections can be programmed to implement simple analog functions. Programmable interconnect networks route signals around CABs to realize more sophisticated analog functions. I/O circuits provide interface between FPAA internal circuits and outside systems. Finally, on-chip memories are used to store all configuration data (configuration bitstream) of the FPAA chip.

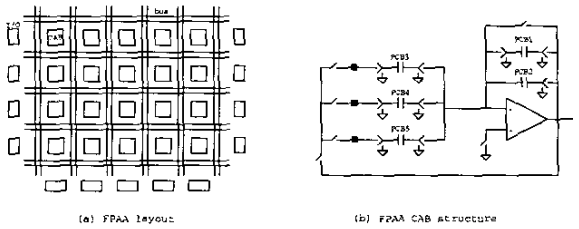


Figure 1. An FPAA structure [24].

There are various circuit techniques to implement FPAA circuits [1]. Among them, switched-capacitor (SC) technology is particularly attractive in the design of FPAAs. This is mainly because SC circuits have high accuracy, are insensitive to parasitics, and can be easily programmed. As an example, Figure 1 shows an SC-based FPAA architecture [24, 25] which was produced by Motorola. A modified version of this FPAA architecture is currently produced by Anadigm, Inc [4]. As shown in Figure 1, this architecture contains 20 CABs, arranged into a 4×5 array. Around the three sides of the CAB array, there are 13 I/O circuits. Each CAB consists of an operational amplifier (OA), five programmable capacitor banks, and a number of switches. The values of capacitor banks as well as the states of switches can be configured to implement different functions. Since SC circuits are discrete-time circuits by nature, exact circuit analysis for SC-based FPAAs should be performed in Z domain. However, when signal frequencies are significantly smaller than (e.g. smaller than one-tenth of) the clock frequencies of SC circuits, FPAA circuits can be approximately treated as continuous-time circuits and, hence, their operations can be analyzed in S domain. With this approximation, a capacitor with its associated switches in the above CAB can be programmed into a capacitor, positive resistor, or negative resistor. The configurations for realizing these three types of components are described in Figure 2. When a resistor (both positive and negative) is configured, the absolute value of the resistance is given by:

$$R = \frac{T}{C} \tag{1}$$

where, T is the period of the clock in the FPAA circuit and C is the capacitor value. In the rest of the paper, we will treat all the circuits implemented on SC-based FPAAs as continuous-time circuits. Also, we will use conventional resistor and capacitor symbols to represent circuits shown in Figure 2(b), (c), and (d).

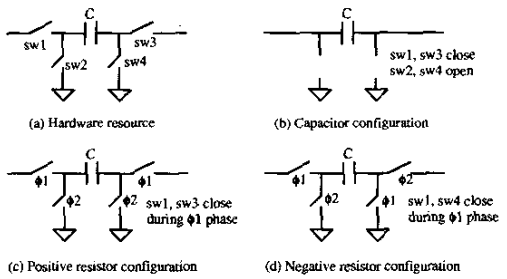


Figure 2. Programming hardware resources in CABs.

2.2 On-line testing FPAA circuits

Many of the latest FPAA devices support partial dynamic reconfiguration; which allows parts of FPAA circuits to be reconfigured on-the-fly without disturbing the operation of the rest of the circuit. Such devices provide an ideal platform to implement redundancy-based on-line testing circuits. Figure 3 shows how the proposed on-line testing method is applied to an analog circuit that consists of a gain stage and two filter circuits. To test the gain stage, a part of the testing module is configured to duplicate the gain stage. The duplication circuit has the same input as the original circuit. The outputs of the two circuits are compared by a comparator. If there are no faults in the original and testing circuits, the original circuit and its replication should have the same output value (or the difference between the two outputs should be within a small tolerance range). However, if there are faulty components in either the original or the testing circuit, the outputs of

the two circuits will potentially exhibit large difference and, consequently, trigger the output of the comparator swinging away from its normal value to indicate the occurrence of faults. In this work, we propose to partition FPAA circuits according to their implementation and each partitioned sub circuit only takes a single CAB. The primary reason for selecting this type of partition is to minimize hardware overhead of the testing module. By this partition approach, the testing module needs only two CABs. One is for duplicating the sub circuit under test and the other CAB is used to implement the comparator.

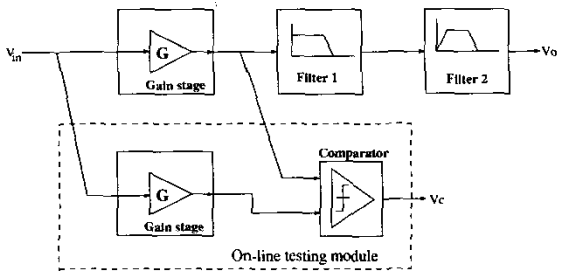


Figure 3. On-line testing scheme for FPAA circuits.

To take advantage of dynamic reconfiguration, the on-line testing module can be programmed to duplicate and test different portions of the circuit at different time. By sharing the same testing module, we not only reduce hardware cost but also potentially save power consumption. In this approach, one important issue needs to be addressed is the problem caused by circuit initial conditions when connecting the testing module to different portions of the CUT on-the fly. For SC-based FPAAs, if the operational amplifiers used in the FPAAs have large slew rate, the impact to the CUT caused by adding the testing module is negligible. However, the testing module does need certain settling time to solve the problem caused by circuit initial conditions. To address this issue, we can use some mechanisms to ignore the comparator output during the settling time period of the testing module.

This on-line testing mechanism also naturally locates faulty circuit blocks when it sequentially tests different blocks of the circuit. Once circuit faults are located, the faulty blocks can be replaced by other fault-free resources on FPAAs through partial reconfiguration. This will lead to analog circuits with self-repairing capability. Another dimension of freedom provided by this on-line testing method is the ability to apply different testing schedules to perform trade-offs between system reliability and power consumption. Use the circuit shown in Figure 3 as an example. On one testing schedule, we can repeatedly test all the three blocks of the circuit without leaving the testing module any idle time. This schedule achieves the maximum reliability but may consume significant power. On another testing schedule, we may test all the blocks once and then shut down the testing module for a certain period of time before we repeat the whole process again. This schedule sacrifices reliability but reduces power consumption. With the help of simple digital circuits, such trade-offs can be easily performed with this on-line testing method.

This on-line testing methodology is not only suitable for FPAA circuits, but also potentially applicable to conventional analog circuits. In such scenarios, a small programmable circuit is used as the testing module to duplicate different portions of conventional analog circuits. One technical challenge in such applications is how to overcome performance mismatches between conventional analog circuits, which are carefully optimized for specific functions, and the programmable module which has to be flexible enough to implement various analog functions. To address this problem, new comparison methodologies need to be developed.

3 Proposed circuit technique for FPAA on-line testing

In the implementation of the above testing method, we have to take circuit stability into consideration. This is because circuit blocks duplicated by the testing module may have unstable transfer functions, which have non left-half-plane poles. Such circuit blocks are stable when they are embedded in the original circuit, due to global feedback in the original circuit. However, there are no feedback loops associated with the replication circuit as shown in Figure 3. Thus, any disturbance or small mismatches between the original circuit and its replication will cause the output of the replication circuit oscillation or saturated, consequently invalidating the testing result. A similar problem has been addressed in literature [13] for on-line testing SC ladder filters. The solution proposed in [13] is shown in Figure 4. A feedback path is added into the on-line testing

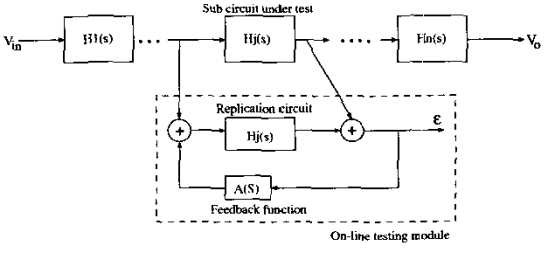


Figure 4. On-line testing circuit proposed in [13].

circuit. The feedback function $A(S)$ is carefully selected such that all the poles of the close-loop circuit are located in the left-half side of the s-plane. Although this technique can be applied in FPAA on-line testing circuits, it normally results in large on-line testing modules and consequently increases implementation cost. In this paper, we propose a more cost-effective alternative to address circuit stability problems. Our technique is explained using the following example. In Figure 5, the sub circuit under test (circuit in the top rectangle) has a pole located at the origin of the s-plane. Instead of simply replicating the original

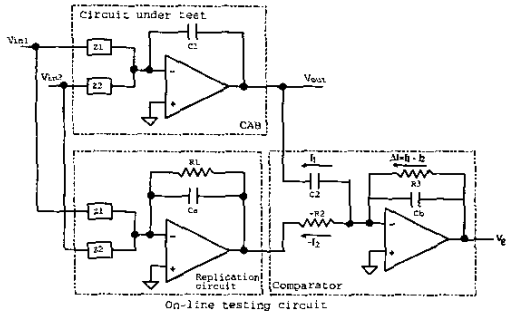


Figure 5. FPAA on-line testing circuit

circuit, we change the amplifier feedback component from a capacitor (C_1 in the original circuit) to a resistive component R_1 in the replication circuit. On SC-based FPAA circuits, R_1 can be implemented as shown in Figure 2(c). With that implementation, the amplifier feedback path in the replication circuit is broken during ϕ_2 clock phase (refer to Figure 2(c)). To address this problem, a small capacitor C_a is added into the amplifier feedback path. The value of C_a is selected small enough such that its impact on the circuit transfer function is negligible. Since the sub circuit under test and its counterpart in the testing module are not exactly the same, conventional comparator circuits cannot be used to compare their outputs. In the proposed comparator circuit, voltage-mode inputs are first converted into current-mode signals. Such conversion is accomplished by using the same type of components that are used in amplifier feedback in the original circuit and its counterpart in the testing module. For example, in Figure 5 capacitor C_1 is used in the amplifier feedback path of the original circuit. In the comparator circuit, capacitor C_2 converts the output of the original circuit into current signal I_1, whose value is given by:

$$I_1(s) = \frac{C_2}{C_1} \cdot \left(\frac{V_{in1}(s)}{Z_1(s)} + \frac{V_{in2}(s)}{Z_2(s)}\right) \tag{2}$$

If $C_1 = C_2$, the above equation can be simplified as:

$$I_1(s) = \frac{V_{in1}(s)}{Z_1(s)} + \frac{V_{in2}(s)}{Z_2(s)} \tag{3}$$

Similarly, negative resistor R_2, whose implementation is shown in Figure 2(d), converts the output of the replication circuit into current signal I_2. If $|R_1| = |R_2|$, then we have:

$$I_2(s) = -\frac{V_{in1}(s)}{Z_1(s)} - \frac{V_{in2}(s)}{Z_2(s)} \tag{4}$$

The comparator output V_ϵ can be expressed as:

$$V_\epsilon(s) = (I_1(s) + I_2(s)) \cdot R_3 \tag{5}$$

Note that capacitor C_b in the comparator circuit is another small capacitor for stabilizing the output of the amplifier when the resistive feedback path is broken. Its effect is neglected in the above analysis. If no faults occur in the circuit, I_1 should equal $-I_2$. Therefore, the comparator output should be zero. On the contrary, if there are faults, I_1 will differ from $-I_2$. The comparator circuit will amplify the current difference and its output will indicate the occurrence of faults. Although the above discussion is based on a simple circuit that contains only one amplifier, the proposed technique can be easily applied to complex circuits with multiple amplifiers if there are no global feedback loops in the sub circuit to be replicated. Global feedback loops stand for circuit loops that contain more than one operational amplifiers. Sub circuits with global feedback normally have stable transfer functions due to their feedback loops. Therefore, such circuits can be simply duplicated.

Note that the use of negative resistors dramatically simplifies the comparator circuit. However, negative resistors also bring certain inaccuracy into the testing results, especially when signal frequency is high. A detail analysis of the error caused by negative resistors is given in [26]. Also, a desirable property for comparators (or checkers) used in analog testing is the capability to adjust their threshold voltages (or tolerance ranges) according to the magnitude of circuit outputs [27, 28]. By taking advantage of dynamic reconfiguration, such property can be obtained for FPAA comparators. Furthermore, for the purpose of identifying if faults occur at the CUT or the testing module, it is preferred to have testing circuits with self-testing capability [29, 17]. To achieve this feature on FPAA testing circuits, a two-phase testing mechanism can be implemented. In the first phase, the testing module is configured to test itself. Then, during the second phase the testing module is connected to test the CUT.

4 Impact of circuit partition on testability

In the proposed on-line testing approach, FPAA circuits need to be partitioned into sub circuits. This section investigates how circuit testability is affected by performing circuit partition. In this discussion, we focus on detecting parametric faults since catastrophic faults are relatively easy to be detected. Also, our analysis concentrates on single-fault scenarios. Conclusions drawn from this discussion can be applied to multi-fault scenarios in most practical cases. In the following discussion, we first derive a formula to estimate circuit testability. Then, we conduct our investigation targeting analog circuits without and with global feedback.

Assume a partitioned sub circuit has the following transfer function:

$$V_o(s) = \sum_i H_i(s) \cdot V_i(s) \tag{6}$$

We use $V_o(s)$ to denote the output of the sub circuit. $V_i(s)$ represents the ith input of the circuit. With the assumption that all the circuits under consideration are linear circuits, we use $H_i(s)$ to represent the transfer function from

the ith input to the output of the circuit. In addition, we use $V_o^R(s)$ and $H_i^R(s)$ to denote the counterparts of $V_o(s)$ and $H_i(s)$ in the replication circuit. To construct a single parametric fault scenario, we assume that the value of a component is changed by $a\%$. As a result, there will be a difference, denoted as $\Delta V(s)$, between $V_o(s)$ and $V_o^R(s)$. We use $\Delta V(s)/V_o(s)$, instead of $\Delta V(s)$, as the figure of merit to measure the testability of the circuit. This is explained as follows. For a given $\Delta V(s)$ value, if $V_o(s)$ is large, a small percentage variation on $V_o(s)$, which is due to normal component mismatches or other environmental factors, may be large enough to conceal $\Delta V(s)$. However, for the same $\Delta V(s)$ value, if $V_o(s)$ is small, the same percentage variation on $V_o(s)$ may not mask $\Delta V(s)$. Thus, it is difficult to detect a small voltage difference caused by a parametric fault when the normal output of the circuit is large.

The value of $\Delta V(s)/V_o(s)$ can be calculated as:

$$\begin{aligned}\frac{\Delta V(s)}{V_o(s)} &= \frac{1}{V_o(s)}(V_o^R(s) - V_o(s)) \\ &= \frac{1}{V_o(s)}\sum_i (H_i^R(s) - H_i(s)) \cdot V_i(s) \\ &= \frac{1}{V_o(s)}\sum_i \Delta H_i(s) \cdot V_i(s) \end{aligned} \quad (7)$$

$\Delta H_i(s)$ is the variation on $H_i(s)$ due to the parametric fault. In the first order approximation, $\Delta H_i(s)$ can be estimated by:

$$\begin{aligned}\Delta H_i(s) &= \frac{\partial H_i(s)}{\partial X} \cdot \Delta X \\ &= \frac{\partial H_i(s)}{\partial X} \cdot \frac{a}{100} \cdot X \end{aligned} \quad (8)$$

where, X is the variable representing the value of the component in which the parametric fault occurs. Substituting Equation 6 and 8 into Equation 7, we have:

$$\frac{\Delta V(s)}{V_o(s)} = \frac{a}{100} \cdot [\frac{X}{\sum_i H_i(s) \cdot V_i(s)} \cdot \sum_i \frac{\partial H_i(s)}{\partial X} \cdot V_i(s)] \quad (9)$$

If the sub circuit under test has a single input and a single output (SISO), the term in the bracket of the above equation becomes the logarithmic sensitivity [30] of the analog function implemented on the sub circuit. Thus, Equation 9 implies that for SISO circuits the testability of a parametric fault on component X is proportional to the sensitivity of the network function with regard to component X. This conclusion is obviously true for single-input analog functions. In the above analysis, we assume the sub circuit under test is directly duplicated and voltage-mode signals are monitored by a comparator. If the sub circuit under test is not a stable circuit, circuit techniques described in Section 3 will be used and, consequently, current-mode signals will be monitored. For these scenarios, similar conclusions can be obtained.

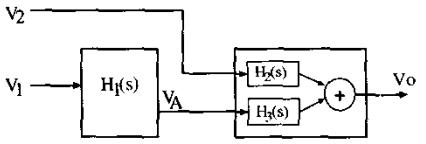


Figure 6. Simplified model for analog circuits without feedback paths.

For analog circuits without global feedback, we can use the simplified model shown in Figure 6 to study the impact of circuit partition on testability. Although the model contains only two blocks and has two inputs, the analysis result obtained from this model illustrates the general principles that are also true for more complex circuits. Assume the value of component X is changed by $a\%$ due to a parametric fault in the first sub circuit, which has a transfer function $H_1(s)$. If we duplicate the entire circuit in the testing module and compare $V_o(s)$ with the output of the replication circuit, the testability measured by $\frac{\Delta V(s)}{V_o(s)}$ can be calculated using Equation 9.

$$\frac{\Delta V(s)}{V_o(s)} = \frac{a}{100} \frac{H_3(s)\frac{\partial H_1(s)}{\partial X} V_1(s) \cdot X}{H_3(s) \cdot H_1(s) \cdot V_1(s) + H_2(s) \cdot V_2(s)} \quad (10)$$

However, if we perform circuit partition in the testing process, then only sub circuit $H_1(s)$ is duplicated in the first testing phase. In this case, the testability is measured by:

$$\begin{aligned}\frac{\Delta V(s)}{V_A(s)} &= \frac{a}{100} \frac{\frac{\partial H_1(s)}{\partial X} V_1(s) \cdot X}{H_1(s) \cdot V_1(s)} \\ &= \frac{a}{100} \frac{\frac{\partial H_1(s)}{\partial X} \cdot X}{H_1(s)} \end{aligned} \quad (11)$$

Comparing Equation 10 and 11, we conclude that circuit partition degrades testability only if the magnitude of $H_3(s) \cdot H_1(s) \cdot V_1(s) + H_2(s) \cdot V_2(s)$ is smaller than that of $H_3(s) \cdot H_1(s) \cdot V_1(s)$. In other cases, performing circuit partition always increases testability. In the process to generate circuit partitions, transfer functions of analog circuits are available. If the properties (frequencies and phase) of input signals are predictable, the above analysis method can be used to estimate the testability for each circuit partition. By doing this, partitions that severely degrade circuit testability can be avoided.

For analog circuits with global feedback, deriving closed-form expressions for estimating testability will involve extremely complicated equations, making such approach unattractive in practice. Fortunately, most feedback paths in linear analog circuits are negative feedback paths, which make circuits more stable and less sensitive to component mismatches. Partitioning such circuits will frequently break the negative feedback loops in replication circuits. As a result, performing circuit partition as required by the proposed testing methodology will very

likely improve the circuit testability. This is illustrated in the following example. Figure 7(a) shows an SC low-pass Biquad filter. Its corner frequency f_o and quality factor Q are given by:

$$f_o = \frac{1}{2\pi R_4 C_1} \tag{12}$$

$$Q = \frac{R3}{R2} \tag{13}$$

Note that all the resistive components are actually implemented using capacitors and switches as shown in Figure 2. Due to the availability of negative resistors, this Biquad circuit needs only two, instead of three, operational amplifiers. To make $f_o = 20KHz$ and $Q = 1$, we arbitrarily select a set of component assignments as follows: $C_1 = C_2 = 159pf$ and $R_1 = R_2 = R_3 = R_4 = 50K\Omega$ (the corresponding capacitors are $20pf$ with SC clock frequency $f_{clk} = 1MHz$).

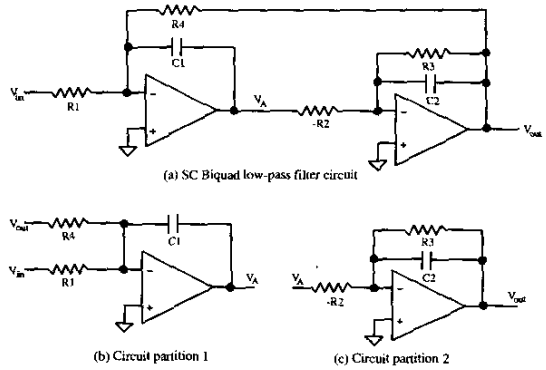


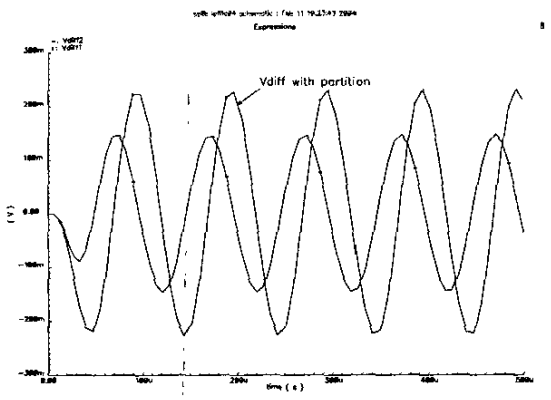
Figure 7. An SC low-pass Biquad filter circuit and its partition

There are two approaches to test this filter circuit. In the first approach, the Biquad circuit is partitioned into two sub circuits which are shown in Figure 7(b) and (c). In each testing phase, only one sub circuit is duplicated and tested. In the second approach, the whole filter circuit is replicated. To investigate the testability in these two approaches, circuit simulation was conducted to compare the proposed figure of merit for testability. In each round of circuit simulation, we injected one parametric fault: reducing the value of the selected component by 20%. The input signal used in simulation is a sine wave with offset voltage 2.5V, frequency 10KHz, and magnitude 1.25V. Although we performed fault simulation for all the six components, due to space consideration Figure 8 shows only the simulation results for the cases that parametric faults occur in components R_3, C_1, and C_2. For each case, both the voltage difference ΔV (or current difference ΔI) and the figure of merit for testability, $\Delta V/V$ (or $\Delta I/I$), are plotted. The testability during the whole simulation period is indicated by the peak absolute value, PAV, of the $\Delta V/V$ (or $\Delta I/I$) curve. The larger the PAV is, the easier is the detection of the parametric fault. Figure 8(a) and (b) compare simulated results for the above two testing approaches when the parametric fault occurs in component R_3. In particular, the left plot shows the voltage difference ΔV. The curve with a label corresponds to the ΔV when circuit partition is performed. From Figure 8(b) which plots $\Delta V/V$, we can see the partitioned approach enjoys a higher PAV of $\Delta V/V$ (0.25 for the partitioned approach versus 0.15 for the un-partitioned approach). The sub circuit shown in Figure 7(b) is not a stable circuit by itself. Thus, the technique proposed in Figure 5 has to be used in the partitioned approach. Instead of comparing voltage-mode signals, current-mode signals are monitored when the sub circuit shown in Figure 7(b) is being tested. For the case that a parametric fault occurs in C_1, the simulated ΔI in the partitioned approach and ΔV in the un-partitioned approach are shown in Figure 8(c). The top curve is ΔV, ranging from -200mV to 100mV. The bottom curve represents ΔI, which is within a range from -4uA to 3uA. To compare testability, the corresponding $\Delta I/I$ and $\Delta V/V$ are plotted in Figure 8(d). The curve at the bottom represents $\Delta I/I$ (it is negative during the entire simulation period). $\Delta I/I$ has a larger PAV (0.25) comparing to $\Delta V/V$, whose PAV is around 0.1. Our simulation results showed partitioning the filter circuit improves the testability for parametric faults on all passive components except C_2. The simulated ΔV and $\Delta V/V$ curves, corresponding to the case that the parametric fault takes place on C_2, are plotted in Figure 8(e) and (f), respectively. It shows the PAV (0.07) of $\Delta V/V$ in the partitioned approach is almost the same as that in the un-partitioned approach.

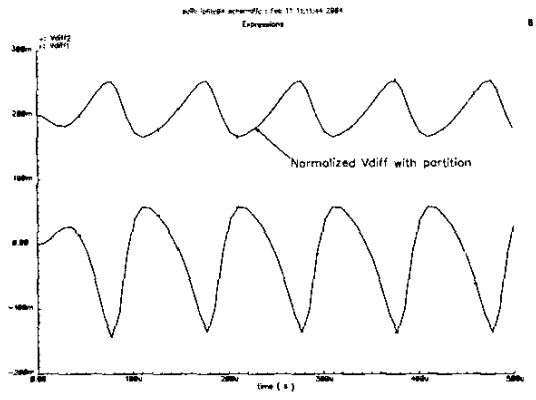
5 Experimental Results

The proposed on-line testing techniques have been demonstrated on a Motorola FPAA chip [25, 24][1]. One of the circuits that we tested is the low-pass Biquad filter circuit shown in Figure 7(a). In our experiment, we used the same component assignments as the simulation setup. The filter input was also a sine wave with frequency 10KHz, magnitude 1.25V, and offset voltage 2.5. We partitioned the circuit as shown in Figure 7(b) and (c). When testing the sub circuit in Figure 7(b), the comparator shown in Figure 5 was used. Meanwhile, a subtractor amplifier circuit [25], which can be implemented by a single CAB, was used as the comparator to test the sub circuit in Figure 7(c). In the experiment, if the peak-to-peak value of the comparator output exceeds 1V, the fault is detected. Otherwise, the testing circuit fails to detect the fault. Also, only one fault was injected (by programming the capacitor to an incorrect value) in each experiment. Figure 9 shows

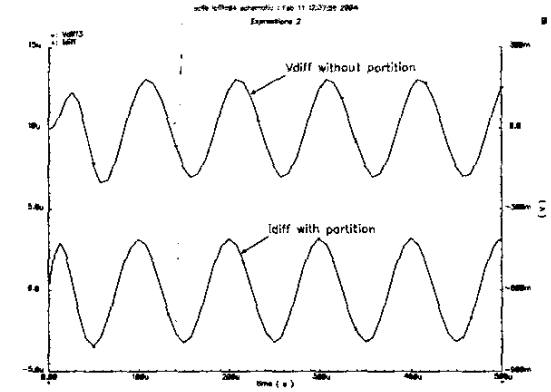
[1]Since the FPAA used in our experiments is an early product, it does not support partial dynamic reconfiguration. Therefore, each time when we reprogram the testing module, the operation of the entire circuit will be suspended for loading the configuration bitstream into the chip. This problem will be fully solved by using new FPAA devices that support partial dynamic reconfiguration.



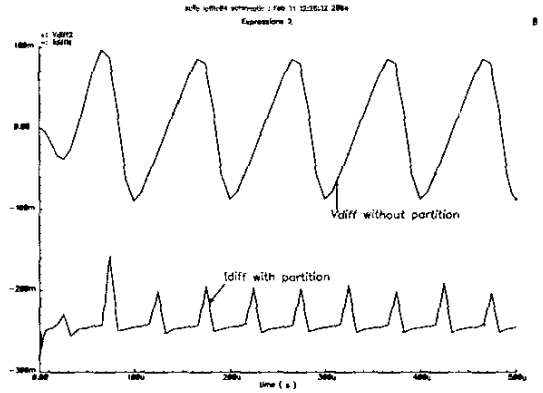
(a) ΔV with faulty R_3



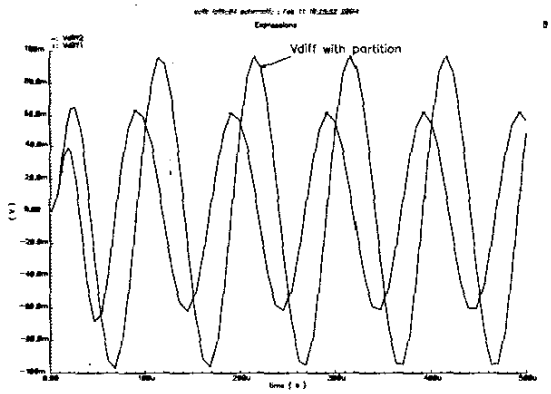
(b) $\Delta V/V_o$ with faulty R_3



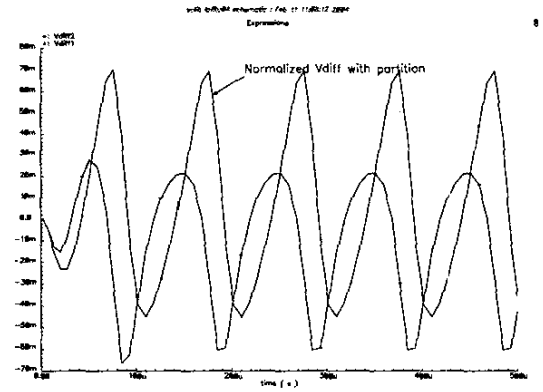
(c) ΔV and ΔI with faulty C_1



(d) $\Delta V/V_o$ and $\Delta I/I$ with faulty C_1



(e) ΔV with faulty C_2



(f) $\Delta V/V_o$ with faulty C_2

Figure 8. Testability comparison for circuits with and without partition.

the captured comparator output when the value of R_1 is decreased by 10% due to a parametric fault. The comparator output is the top curve in the oscilloscope screen. It has a peak-to-peak value of 1.38V. The bottom curve is the filter output when the fault occurs. Since this parametric fault slightly changes the filter corner frequency, the input signal is still passed to the filter output without significant attenuation.

With the above experiment setup, the smallest detectable parametric faults for the filter circuit are summarized in Table 1. The second column of the table lists the capacitor and resistor values in the fault-free filter circuit. The third column gives the actual capacitor values (in terms of unit capacitance on the FPAA chip) that are used to implement the corresponding component values listed in the second column. The fourth column documents the smallest detectable faults in the scenarios that capacitor values increase due to the existence of faults. Such type of faults are referred to as value-increase faults. The smallest detectable faults are described in terms of the percentages of capacitance variation due to the faults. For example, Table 1 shows the smallest detectable value-increase fault for

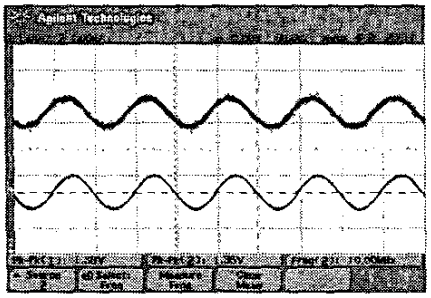


Figure 9. Captured comparator output.

R_1 is 15%. It means that our experiment detected the parametric fault which changes the value of the capacitor corresponding to R_1 from 20 to 23. The smallest detectable value-decrease faults, which decrease the corresponding capacitor values, are summarized in the fifth column of the table. Note that the smallest detectable value-increase and value-decrease faults do not exhibit the same percentage of variation. This is because changes of component values in different directions may affect the circuit behavior with different levels of sensitivity. Also, it is noted that parametric faults on capacitor C_2 are most difficult to be detected. This coincides with our early simulation results.

Table 1. Smallest detectable parametric faults in low-pass Biquad filter circuit.

	Equivalent Comp. values	FPAA Cap. values	Value-Inc. faults	Value-dec. faults
R_1	$50K\Omega$	20	15%	10%
R_4	$50K\Omega$	20	10%	10%
C_1	$159pf$	159	12%	18%
R_2	$50K\Omega$	20	15%	15%
R_3	$50K\Omega$	20	15%	20%
C_2	$159pf$	159	45%	21%

In addition to Biquad filters, we also successfully tested other types of circuits. Table 2 lists our experimental results on testing a low-pass leapfrog filter circuit [30]. The schematic of the filter is given in Figure 10. It implements a third-order Chebyshev filter whose pass-band is at 10KHz. The filter input during our testing operation was a 5KHz sine wave signal with the peak-to-peak magnitude of 1.25V. In this FPAA circuit, programmable capacitors are either programmed to the largest feasible capacitance value (255) or configured close to the smallest capacitor value (1). This fact poses constraints on the selection of comparator component values, and consequently limits the optimization space in comparator design. This mainly explains why the smallest detectable parametric faults for many components are larger than that in the previous Biquad circuit. In addition, other factors, such as component sensitivities and circuit non-ideal effects, may also contribute to the degraded testability in the leapfrog circuit. How to minimize the effect of such factors will be addressed in our future study.

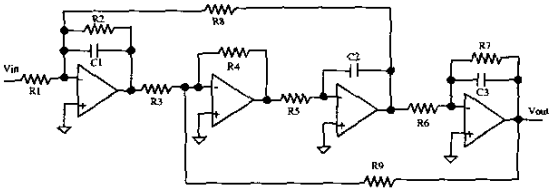


Figure 10. A low-pass leapfrog filter.

Table 2. Smallest detectable parametric faults in the low-pass leapfrog filter circuit.

	Equivalent Comp. values	FPAA Cap. values	Value-Inc. faults	Value-dec. faults
R_1	$125K\Omega$	8	13%	13%
R_2	$125K\Omega$	8	13%	13%
R_8	$125K\Omega$	8	13%	13%
C_1	$255pf$	255	N/A*	10%
R_3	$125K\Omega$	8	38%	50%
R_4	$125K\Omega$	8	63%	38%
R_9	$125K\Omega$	8	38%	25%
R_5	$125K\Omega$	8	150%	38%
C_2	$125pf$	125	52%	56%
R_6	$125K\Omega$	8	25%	25%
R_7	$125K\Omega$	8	25%	13%
C_3	$255pf$	255	N/A*	18%

* C_1 and C_3 were programmed to the maximum feasible capacitor value. Therefore, we could not increase these capacitor values in our experiment to find detectable value-increase faults for C_1 and C_3.

In our experiments, example circuits are relatively low frequency circuits. This is mainly due to the performance limitation of the FPAA device. For high frequency applications, circuit will be more vulnerable to parasitic effects. However, with careful circuit design, this FPAA on-line testing method should be able extend to high frequency domain. Although example circuits presented here are relatively small, the method should work with large circuits since we always partition circuits under test into sub circuits that occupy single CABs. The size of the circuits should not affect the validity of the testing method. This work primarily focuses on linear circuits. In future, we will extend this method to nonlinear circuits. Consequently, we will conduct experiments with nonlinear circuits, such as ADC or DAC circuits. A limitation in our experiment is the selection of input signals. We always use sine waves when conducting circuit testing. In practical cases, circuit inputs can be arbitrary signals, and properties of input signals potentially affect the testing results. This raises an interesting question for this testing method: *what is the confidence level of the testing result for a given statistical characteristics of the input signals?*. As the future work of this study, we will conduct experiments with different types of input signals and investigate the confidence level of the testing results from theoretical aspects.

6 Concluding Remarks

In this work, we presented a methodology to on-line test field programmable analog array circuits. Also, we developed circuit techniques to address stability problems that are often encountered in the proposed testing method. Circuit analysis and simulation have been conducted to investigate how circuit testability is affected by performing circuit partition as required in the proposed method. A closed-form formula is developed to estimate testability for analog circuits without global feedback. Additionally, our simulation results indicate that partitioning analog circuits with negative feedback normally increases circuit testability. Finally, we presented experimental results to demonstrate the feasibility of the developed techniques.

The proposed on-line testing method has many advantages and can be used in various applications. Because of the use of programmable testing circuits and performing circuit partition, this approach enjoys low implementation cost, enhanced circuit testability, and flexible testing schedules which can be exploited to fit different reliability and power consumption constraints. Since fault-diagnosis capability comes quite naturally to this on-line testing method, the proposed testing approach can also be used to locate faulty circuit blocks on FPAA circuits. After faulty blocks are identified, FPAA circuits can be reconfigured to replace faulty circuits. This leads to analog circuits with fault-recovery capability. Another promising application of the developed techniques is to integrate a programmable testing module with conventional analog ICs. By following similar procedures, the programmable module can be configured to test different portions of the conventional analog circuits.

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