Southern Illinois University Carbondale
OpenSIUC

Conference Proceedings

Department of Electrical and Computer Engineering

12-1995

The Related Effects of Increased PN Junction Area on ESD Protection Capability

Po-ching Liu
Nanyang Technological University, Singapore

Brian Lee
Nanyang Technological University, Singapore

Eng Aik Lian
Nanyang Technological University, Singapore

Gan Cheong Hock
Nanyang Technological University, Singapore

Haibo Wang
haibo@engr.siu.edu

Follow this and additional works at: http://opensiuc.lib.siu.edu/ece_confs

Published in Liu, P.C., Lee, B., Lian, E.A., Hock, G.C., & Wang, H. (1995). The related effects of increased PN junction area on ESD protection capability. Proceedings of the 1995 5th International Symposium on the Physical and Failure Analysis of Integrated Circuits, 116-120. doi: 10.1109/IPFA.1995.487607 ©1995 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE. This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.

Recommended Citation

Liu, Po-ching; Lee, Brian; Lian, Eng Aik; Hock, Gan Cheong; and Wang, Haibo, "The Related Effects of Increased PN Junction Area on ESD Protection Capability" (1995). *Conference Proceedings*. Paper 38.
http://opensiuc.lib.siu.edu/ece_confs/38

This Article is brought to you for free and open access by the Department of Electrical and Computer Engineering at OpenSIUC. It has been accepted for inclusion in Conference Proceedings by an authorized administrator of OpenSIUC. For more information, please contact opensiuc@lib.siu.edu.

THE RELATED EFFECTS OF INCREASED PN JUNCTION AREA ON ESD PROTECTION CAPABILITY

Liu Po-ching, Brian Lee, Eng Aik Lian, Gan Cheong Hock, and Wang Haibo

School of Electrical and Electronic Engineering

Nanyang Technological University

Singapore 2263

Abstract

ESD protection devices comprising polysilicon resistor, Vcc and Vss connected diodes with different sizes of PN junction area were fabricated on CMOS test chip and underwent ESD stress. The result of testing shows that larger PN junction area will subject the polysilicon resistor to bear more energy from ESD stress and end up with more failures. The relationship between stressing energy and junction area is hereby derived. Different failing modes for positive and negative ESD pulses are also identified. By comparing our own design with those of commercials, a safe length of contacting parameter at Al-Polysilicon contact capable of handling the discharging current is identified to be more than 90μm.

I Introduction

A test chip (RASRAM) was fabricated by 1.2μm N-well process as shown in Fig.1. Some of the test structures were designed to evaluate the effect of PN junction area on the performance of ESD protection device consisting of polysilicon resistor, Vcc-connected and Vss-connected diodes as shown in Fig.2 [1].

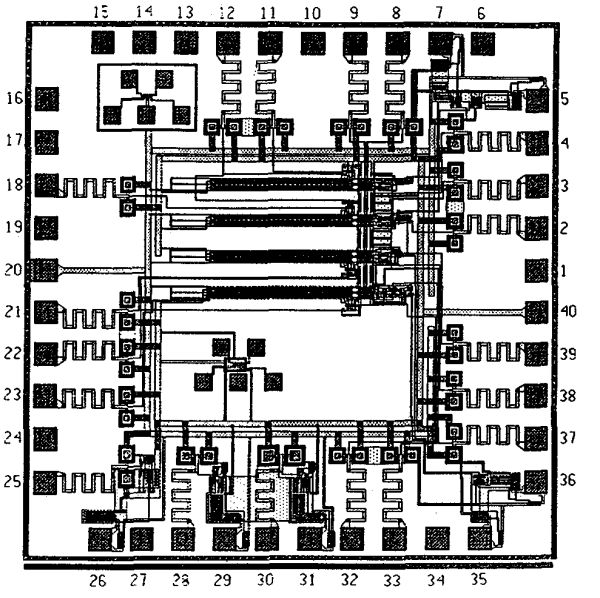


Fig.1 Layout of the RASRAM test chip.

In contrary to the conventional thinking that large PN junction area will carry and tolerate more discharging current, thus offering larger ESD threshold voltage, the device actually performed in the opposite manner. With larger PN junction area, the internal node (node A in Fig. 2) will absorb most of the discharging energy during the initial ESD surge. The polysilicon resistor will then dissipate more energy from high voltage stressing and generate more joule heating , thus more liable to burning.

0-7803-2797-7/95/$4.00©1995 IEEE

Authorized licensed use limited to: Southern Illinois University Carbondale. Downloaded on May 28, 2009 at 18:12 from IEEE Xplore. Restrictions apply.

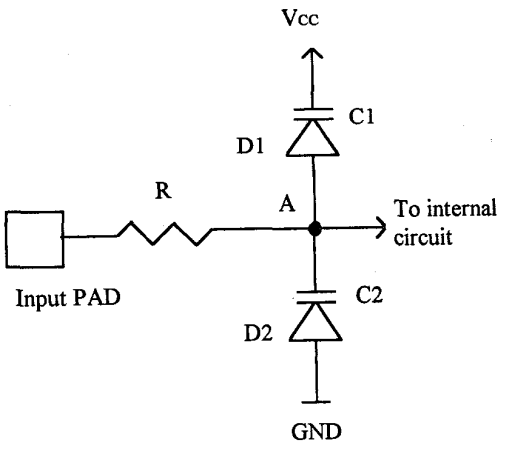


Fig. 2 ESD input protection circuit.

In this test chip, three different sizes of junction area are incorporated. Four pieces of the RASRAM test chip were subjected to HBM ESD stress. The evidence of damages at turning corners of the polysilicon resistor due to positive ESD stress and the initial metal-to-polysilicon contact hole due to negative ESD stress are produced. Statistical data for the failure voltage of input pins in different testing conditions are cited in this paper. A simple relationship between stressing energy and PN junction area is also derived. The appropriate perimeter length of the initial contact hole capable of carrying nominal ESD discharging current is obtained by comparing our own design with two other standard commercial parts.

II Description of Test Chip

The RASRAM test chip was designed and fabricated by 1.2 μm CMOS N-well process supported by Orbit Semiconductor. The test chip was designed for testing different sensing schemes for CMOS SRAM. The ESD protection circuit consisting of a polysilicon resistor and a pair of protection diodes is incorporated at every input pin. In total there are 19 input pins with three different sizes of protection diodes. The dimensions and estimated junction capacitance are shown in Table 1.

III ESD Testing

Four pieces of the RASRAM test chip were subjected to HBM ESD stress. The test is according to MIL-STD-883C Notice 8 Method 3015.7. The pin-under-test was subjected to repetitive pulses (three pulses) at the same voltage supplied by IMCS 700 ESD simulator. Measurements were made on HP4145A semiconductor parameter analyzer. The interval between pulses was set at one second. ESD threshold voltage level and leakage current were recorded at every incremental step for each input and output pin. This procedure continued until either failure occurred or the test equipment maximum voltage was reached. Four pieces of the RASRAM test chip were subjected to ESD stress. The test was conducted as follows:

(i) Two pieces stressed with all unused pins grounded.
(ii) One piece stressed with respect to ground pin.
(iii) One piece stressed with respect to Vcc pin.

A summary of the failure voltage of input pins for different testing conditions is shown in Table 2. It is seen that the polysilicon resistor and initial contact hole for input with larger protection diodes (medium and large junction area) generally failed at lower ESD voltage.

From the results illustrated in Fig. 3 and Fig.4, we found that with positive ESD pulses, the main cause of failure is due to the burning of polysilicon resistor, especially at the turning corners. This accounts for 33 out of 39 failures on burnt polysilicon resistor. Whereas, when the device is zapped with negative ESD pulses, the

Authorized licensed use limited to: Southern Illinois University Carbondale. Downloaded on May 28, 2009 at 18:12 from IEEE Xplore. Restrictions apply.

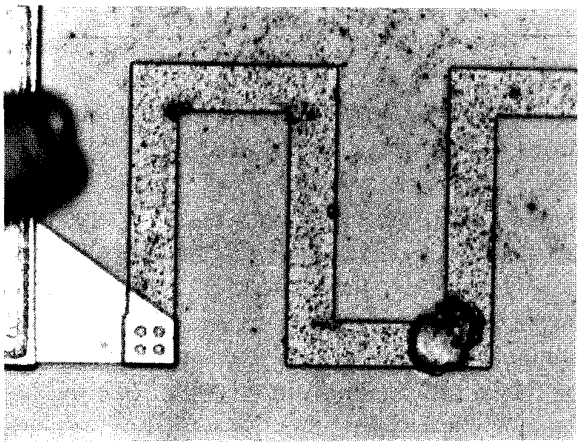


Fig. 3 Polysilicon resistor with burnt corner.

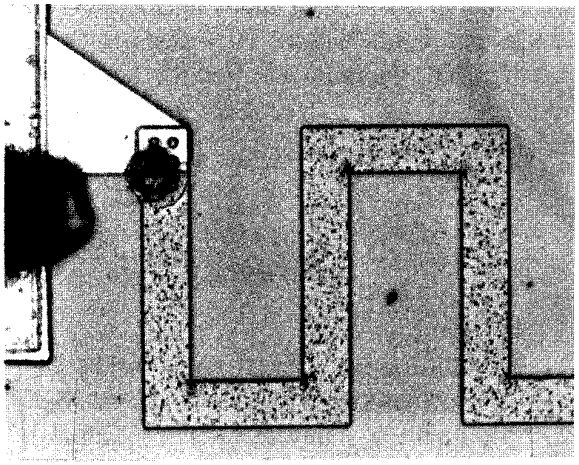


Fig. 4 Polysilicon resistor with burnt metal-polysilicon contact.

main cause of failure is due to the burning of metal-to-polysilicon contact hole nearby the bonding pad. This accounts for 34 out of 41 failures located at the contact regions.

To identify the safe size (or perimeter length) of the initial contact hole, a comparison was made among 74HCT00 (fast CMOS logic element), HM6264LP (64K CMOS SRAM) and the RASRAM test chip. The result is summarized in Table 3. We found that the contact-hole size used in the RASRAM test chip is considerably smaller than the established commercial parts.

IV Discussions

The dependence of the failing mode of protection devices (shown in Fig.3 & Fig.4) on the polarity of ESD pulses can be explained as follows:

When positive ESD pulses are applied to the input pins, electrons will rush out from the polysilicon resistor to the bonding pad. At the turning corners of the polysilicon resistor, the electric field is unduly high, ending with high current density, thus failures caused by positive ESD pulses tend to concentrate on the sharp corners of polysilicon resistor. With negative ESD pulses applied at the bonding pad, unusually large amount of electrons are driven from bonding pad to the polysilicon resistor through the metal-to-polysilicon contact hole. Since the current is generally understood to flow via the perimeter, undersized contact hole (or perimeter) on the RASRAM test chip is responsible for the failure. With reference to Table 3, the effective contact hole perimeter on the RASRAM test chip (33.30μm) is less than one half of that commercial standard part. A safe length of contact perimeter should be no less than 90μm. Length of 100μm is even better.

The qualitative explanation for the trend of lower ESD threshold voltage is associated with larger junction area can be reasoned as follows:

For a given input ESD voltage, the voltage at node A in Fig.2 will rise slower if the junction area is larger in association with larger junction capacitance. This will subject the polysilicon resistor and related metal-to-polysilicon contact to bear more high voltage stressing. The protection device is therefore more liable to damage with larger junction diodes.

The qualitative picture can be obtained by considering the case when ESD occurs with the device connected to Vcc. We assume a positive

Authorized licensed use limited to: Southern Illinois University Carbondale. Downloaded on May 28, 2009 at 18:12 from IEEE Xplore. Restrictions apply.

device connected to Vcc. We assume a positive ESD pulse is passing through the protection circuit in Fig.2. Initially the voltage of node A is less than (Vcc+VF) with VF being the offset voltage of diodes. The two protection diodes are off and can be regarded as two capacitors C1 and C2 until VA= Vcc+VF. We name this period as period I. After VA= Vcc+VF, D1 turns on and drains the ESD current through the polysilicon resistor to Vcc, diode D1 is then represented by its forward dynamic resistance r. We name this period as period II. Assuming the ESD voltage waveform as step function, The charge introduced by ESD in period I (t_I) is:

$$\Sigma Q = (C_1+C_2)\times(V_{CC}+V_F) \quad (1)$$

The energy (E) introduced by ESD in this period is:

$$E=V_{ESD}\times\Sigma Q = V_{ESD}\times(C_1+C_2)\times(V_{CC}+V_F) \quad (2)$$

The bulk of the energy E will be dissipated in the polysilicon resistor and the related contact hole.

$$E_{ploysilicon} \approx E = V_{ESD}\times(C_1+C_2)\times(V_{CC}+V_F) \quad (3)$$

It is in this period that larger value of C1 and C2 will incur more damage to polysilicon resistor path.

During period II (t_{II}):

$$E_{polysilicon} = \left(\frac{V_{ESD}}{R+r}\right)^2 R\times t_{II} = \left(\frac{1}{1+\frac{r}{R}}\right)^2 \frac{V_{ESD}^2}{R}\times t_{II} \quad (4)$$

The energy dissipated by polysilicon resistor is then independent of junction area. Since the current carrying capability is also limited by the length of perimeter of contact holes, we obtain the suitable value (≥90 μm) by comparing commercial standard part with our own design as shown in Table 3.

V Conclusion

By analyzing the measured results of input protection devices on the RASRAM test chip, we found that positive ESD pulses tend to damage the turning corners of polysilicon resistor due to the out-rushing of electrons from polysilicon to the bonding pad. Whereas negative ESD pulses tend to incur burning at the contact hole nearest to the bonding pad, as electrons are driven from the metal pad through contact hole to the polysilicon resistor. Enlarging the junction area of protection diodes will lower the ESD threshold voltage as more ESD energy sunk into the polysilicon resistor and related contact hole. To withstand nominal ESD current, we conclude that the perimeter of first contact hole adjacent to the loading pad should be 90μm or more.

Reference

[1] M. Mardiguian "Electrostatic Discharge, Understanding, Simulate and Fix ESD problem", Interference Control Technologies, U. S. A., 1986, pp. A.1-A.16

Authorized licensed use limited to: Southern Illinois University Carbondale. Downloaded on May 28, 2009 at 18:12 from IEEE Xplore. Restrictions apply.

Junction Size	Dimension (μm^2)	Number of Input Pins	Total Junction Capacitance, Cj(pF)	
			n-channel	p-channel
Large	40.2×40.2	1	0.8735	0.6046
Medium	28.2×28.2	2	0.4817	0.2981
Small	22.8×22.8	16	0.3417	0.1949

Table 1 Capacitance values of various junction sizes of RASRAM.

Sample	Test Condition	Pad Size	Mean ESD Failure Voltage (Volts)			
			Positive Voltage		Negative Voltage	
			Partial	Final	Partial	Final
Sample I	Zapped with all unused pins grounded	Small	1275	1625	1200	1775
		Medium	1300	1400	-	1200
		Large	1200	1400	-	-
Sample II	Zapped with respect to ground pin	Small	1250	1500	1113	1925
		Medium	1200	1300	1100	1600
		Large	-	-	1200	2000
Sample III	Zapped with respect to Vcc pin	Small	1200	1414	1117	1843
		Medium	1200	1400	1100	1800
		Large	-	1300	-	-
Sample IV	Zapped with all unused pins grounded	Small	1175	1463	1113	2300
		Medium	1200	1400	1000	1900
		Large	-	-	1000	1900

- means that the device is still not damaged when the equipment maximum voltage is reached.

Table 2 Mean failure voltage of input pins at various test conditions.

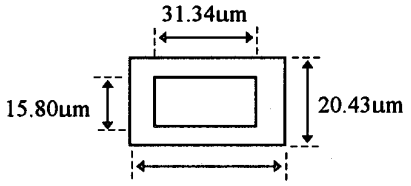
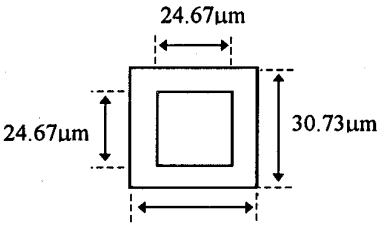
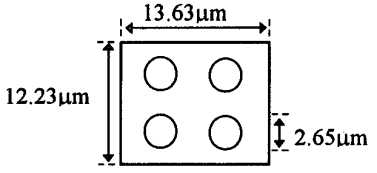
Device	Contact Measurement	Effective Perimeter
74HCT00		94.28μm
HM6264LP		98.67μm
RASRAM		33.30μm

Table 3 Measurement on the perimeters of metal-to-polysilicon contact for three different brands of devices.

Authorized licensed use limited to: Southern Illinois University Carbondale. Downloaded on May 28, 2009 at 18:12 from IEEE Xplore. Restrictions apply.